Pulse Frequency Modulated Interleaved Boost-Integrated LC Series Resonant Converter with Frequency-Free Designed Transformer

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***Abstract*—This paper proposes a novel interleaved boost-integrated LC series resonant converter, in which the series resonant tank is located on the secondary side. Moreover, the input and output of the interleaved boost unit are in series directly, which is helpful to reduce the voltage stress of the output filter capacitor of boost unit. With the proposed pulse frequency modulation, except for that the output voltage can be controlled as constant under different input voltages, another feature is that the high frequency transformer design is related to the series resonant frequency instead of the switching frequency. Hence, the proposed converter can operate under a very wide switching frequency range with a constant maximum magnetic flux density. The zero-voltage-switching and zero-current-switching can be achieved for all switches diodes, respectively. Finally, a 500 W prototype with a switching frequency range from 60 kHz to 200 kHz is built to verify the operation principles of the proposed converter and modulation.**

***Index Terms*—LC series resonant converter, pulse frequency modulation, frequency-free transformer**

I. INTRODUCTION

According to the Renewables 2021: global status report [1], renewable energy sources (RES), such as photovoltaic and fuel cells, have been widely developed and utilized all around the world. The output voltages of them are usually low and have a wide variation range [2]. Hence, a step-up dc-dc converter, which can deal with a wide input voltage range, is required to interface the RES. Thanks to the characteristics of high-power density and high efficiency, the LLC resonant converter is always an attractive candidate [3]-[5].

The traditional LLC resonant converter can employ the traditional pulse frequency modulation (PFM) to meet the wide voltage range demand. However, a wide range of switching frequency will affect the maximum magnetic flux density (MMFD) of the transformer core. Since the MMFD is directly proportional to the volt-second product of the winding voltage and time, which will undoubtedly lead to higher MMFD at the lowest operating switching frequency due to it is always much smaller than the series resonant frequency of the series resonant inductor and the series resonant capacitor of the LLC resonant converter. As a result, the volume and cost of the transformer is increased. Except for the traditional PFM, the fixed frequency control can be adopted for the LLC resonant converter [6], generally including the pulse width modulation (PWM) [7] and the phase-shift PWM [8], where the switching frequency can be set as the same as or slightly lower than the series resonant frequency, and the low MMFD of transformer core can be accordingly obtained [9]. However, to get a wide input voltage, two more switches are employed both in [7] and [8]. In [10], when the series resonant frequency is the same, an asymmetric duty cycle control is proposed for the traditional LLC resonant converter, which reduces the switching frequency by half and maintains the same low MMFD as in [7] and [8]. However, it loses the voltage regulation capability.

To get a lower MMFD for the resonant converter, strenuous efforts have been made and many methods have been proposed. Firstly, the topology reconfiguration, including reconfiguration of the resonant tank, reconfiguration of the primary-side switch network, reconfiguration of the secondary-side rectifier, and the cascaded structure, can be applied to lower down the primary RMS current or improve the light load efficiency [11]-[14]. However, the switching frequency range of them is still relatively wide, and the MMFD is still directly proportional to the volt-second product of the winding voltage and time.

The second method is the mixed control strategies, where the PFM will only function in some certain operation area [16]-[18]. For example in [16], the proposed converter can be PFM regulated when the voltage gain is higher than one, and phase-shift PWM controlled when the voltage gain is lower than one. Similarly, the PFM/phase-shift PWM hybrid modulation is adopted in [17]. As a result, the switching frequency range is narrowed both in [16] and [17]. However, since two full-bridge are adopted, the switch count is doubled. Moreover, the MMFD is still calculated based on the lowest switching frequency, which is relatively lower than the series resonant frequency.

To extend the input voltage range while maintaining low

Manuscript received October 13, 2021; revised January 10, and February 18, 2022; accepted February 28, 2022. This work was supported in part by the Nature Science Foundation of China under Grant 52107219 and Grant 62173351. (*Corresponding author: Guangfu Ning*).

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MMFD, the latest method is the stage-integration [19]-[21], where the first stage of boost unit and the second stage of LLC resonant unit can be integrated into one single stage as interleaved boost-integrated LLC resonant converter. As proposed in [21], the LC series resonant tank is removed from the primary side to the secondary side, where LLC resonant unit is transferred to LC resonant unit. Although the wide input voltage can be realized by the boost unit, the high-frequency transformer still needs to be designed according to the lowest switching frequency. The magnetic flux density (MFD) of LC resonant unit is detailed analyzed in [9], and an asymmetric PFM for LC resonant unit is proposed in [22] to operate with wide voltage range, where the high-frequency transformer can be designed according to the highest switching frequency. In other words, the high-frequency transformer can be frequency-free designed. However, the switching frequency of two switches of the full bridge is doubled, leading to a lower switching frequency upper-limit. In [23], the LC resonant tank is located on the secondary side as in [21], and the named pulse removal technique is proposed to achieve the frequency-free designed transformer. However, it functions as a DC transformer with fixed voltage gain.

To concurrently get a wide switching frequency range and a low MMFD, which is calculated based on the series resonant frequency, an interleaved boost-integrated resonant converter is proposed in this article. Since the resonant tank is located on the secondary side, the resonant capacitor can be rationally designed to guarantee that the resonant capacitor voltage is always lower than the output voltage. Therefore, the primary winding voltage will be clamped to zero after the normal resonance under the proposed PFM, leading to that the volt-second product of the primary winding in the half switching period is constant over the full switching frequency range. Hence, the MMFD is a constant value, which is only related to the series resonant frequency instead of the switching frequency, implying the high frequency transformer is switching frequency independent and can be frequency-free designed. Moreover, since the input and output of the interleaved boost unit are in series directly, the voltage stress of boost unit output filter capacitor can be reduced. At last, the zero-voltage-switching (ZVS) and zero-current-switching (ZCS) can be realized for primary switches and rectifier diodes, respectively.

The rest of this paper is organized as follows. The operation principles of proposed converter are analyzed in Section II. The converter characteristic analysis and parameters design are presented in Section III. A 500 W prototype was set up in the laboratory, and the experimental results are given Section IV for verification. Finally, conclusions are drawn in Section V.

II. Operation Principles

The proposed interleaved boost-integrated LC series resonant converter is as shown in Fig. 1. The primary full-bridge switches Q_1 ~ Q_4 are shared by the LC series resonant converter and the interleaved boost unit (including two boost inductors L_{b1} and L_{b2}), and the secondary side is a full-bridge diode rectifier of D_{R1} ~ D_{R4} with output voltage V_H. The primary and secondary sides are connected by the high frequency transformer T_{hf}, the secondary to primary turns ratio of which is n. Different from the traditional interleaved boost-integrated LLC converter, the resonant tank of resonant inductor L_r and resonant capacitor C_r is put on the secondary side while the magnetizing inductor L_m is still on the primary side. What is more, the filter capacitor C_L of input voltage V_L is multiplexed into the output filter of the interleaved boost unit. Hence, the intermediate voltage V_M is the voltage across the series capacitors C_B and C_L.

The proposed converter is controlled by PFM, and the key waveforms are as shown in Fig. 2. As can be seen, Q_1 and Q_3 are switched out of phase and have the same duty cycle of 50% with enough dead time. The duty cycle of Q_1 and Q_3 is constant under different switching frequency f_s (=1/T_s, the switching period). While Q_4 and Q_2 have the constant on time under different f_s and are controlled on the leading edges of Q_1 and Q_3, respectively. Referring to Fig. 2, the constant on time of Q_4 and Q_2 is just half of the resonant period T_r (=1/f_r, the resonant frequency). As a result, the duty cycle $D_b = 0.5T_rf_s$ of Q_4 and Q_2 will decrease with the decrease of f_s.

Due to the symmetry of the proposed converter and for the simplicity, only the first half switching cycle will be analyzed. Fig. 3 shows the steady states of proposed converter, where there are three modes during the first half switching period. The detailed analysis of each mode is as follows:

1) Mode 1 [t_0, t_1] (see Fig. 3(a)): At t_0, both the currents of Q_1 and Q_4 are negative, hence, the ZVS-on can be achieved for them. Since Q_1 and Q_4 are on during this mode, the voltage v_p across the primary winding of T_{hf} is constant as V_M, and the voltages across L_{b1} and L_{b2} are V_L – V_M and V_L, respectively. Therefore, the current i_{Lb1} of L_{b1} decays linearly while the current i_{Lb2} of L_{b2} increases linearly from I_{Lbmin}, which is the valley value of i_{Lb1} and i_{Lb2}. Hence, i_{Lb1} and i_{Lb2} can be expressed as

$$\begin{cases} i_{Lb1}(t) = i_{Lb1}(t_0) + \dfrac{V_L - V_M}{L_b}(t - t_0) \\ i_{Lb2}(t) = I_{Lbmin} + \dfrac{V_L}{L_b}(t - t_0) \end{cases} \tag{1}$$

where $L_b = L_{b1} = L_{b2}$.

Similarly, the magnetizing current i_{Lm} and the MFD B_t of transformer core increase linearly from –I_{Lmmax} and –B_m, where I_{Lmmax} and B_m is the peak value of i_{Lm} and B_t, respectively. From t_0, C_r starts to forward resonate with L_r, leading to the voltage v_{Cr} across C_r increases from minimum value –V_{Crmax}. Due to the existence of L_m on the primary side, the primary current i_p starts to have a resonance rise from –I_{Lmmax}. The resonant current i_r on the secondary side has a resonance rise from zero, as well as the current of D_{R1} and D_{R4}. In summary, i_{Lm}, v_{Cr}, i_r, and i_p can be expressed as

$$i_{Lm}(t) = \frac{V_M}{L_m}(t - t_0) - I_{Lmmax} \tag{2}$$

$$v_{Cr}(t) = nV_M - V_H - (nV_M - V_H + V_{Crmax})\cos\omega_r(t - t_0) \tag{3}$$

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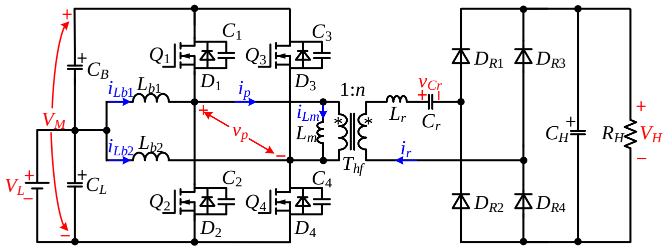

Fig. 1. Proposed converter.

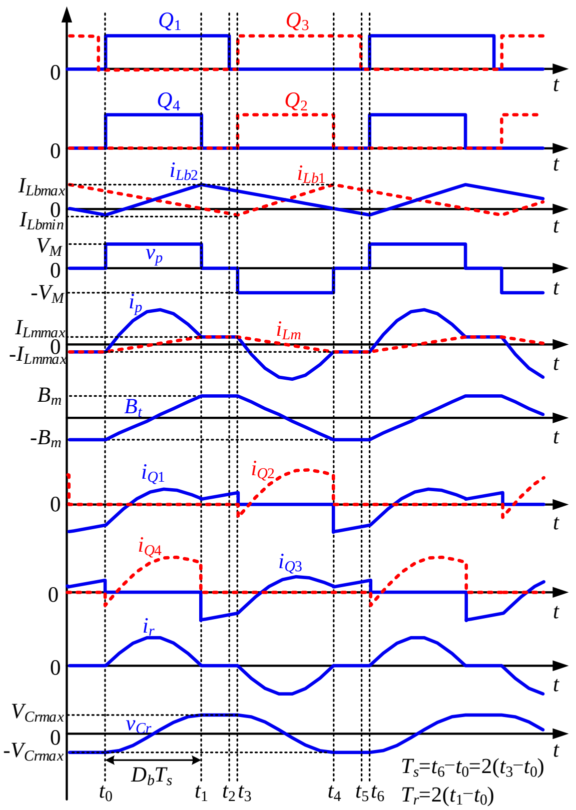

Fig. 2. Key waveforms of the proposed converter under a certain switching frequency.

$$i_r(t)=\frac{nV_M-V_H+V_{Crmax}}{Z_r}\sin\omega_r(t-t_0) \tag{4}$$

$$i_p(t)=ni_r(t)+i_m(t) \tag{5}$$

where

$$Z_r=\sqrt{L_r/C_r},\ \ \omega_r=1/\sqrt{L_rC_r} \tag{6}$$

Furthermore, based on the Faraday law of electromagnetic induction, B_t can be expressed as

$$B_t(t)=\frac{V_M}{N_pA_e}(t-t_0)-B_m \tag{7}$$

where N_p and A_e are the primary winding turn and the effective cross-sectional transformer core area of T_{hf}, respectively.

During this mode, the primary current path includes three parts of two boost units and the LC resonant unit. The discharge current path of i_{Lb1} is ① due to the initial and final values of i_{Lb1} are both positive. The charge current path of i_{Lb2} is from ② to ③ due to the initial and final values of i_{Lb2} are negative and positive, respectively. For the LC resonant unit, i_{Lm} increases linearly while C_r resonates with L_r. In addition, the initial and final values of i_{Lm} are negative and positive, respectively. And i_p is the sum of i_{Lm} and ni_r, therefore, the current path of i_{Lm} and i_p is from ④ to ⑤.

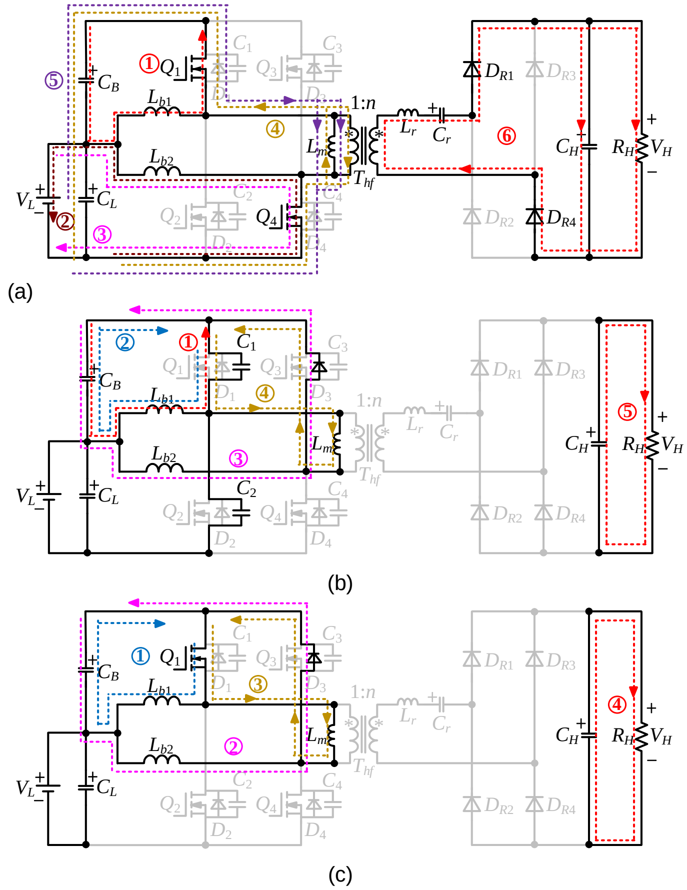

Fig. 3. Equivalent circuits of three modes. (a) [t_0, t_1]. (b) [t_1, t_2]. (c) [t_2, t_3].

2) Mode 2 [t_1, t_2] (see Fig. 3(b)): The forward resonance finishes at t_1, where i_{Lm} (or i_p), v_{Cr}, and B_t come to I_{Lmmax}, V_{Crmax}, and B_m, respectively. Hence, one can obtain

$$I_{Lmmax}=\frac{V_M}{2L_m}(t_1-t_0)=\frac{V_M}{4L_m}T_r \tag{8}$$

$$B_m=\frac{V_M}{2N_pA_e}(t_1-t_0)=\frac{V_M}{4N_pA_e}T_r \tag{9}$$

where the intermediate voltage V_M, the magnetizing inductor L_m, and the resonant period T_r are all constant values, hence, I_{Lmmax} is almost a constant value.

At t_1, i_{Lb2} arrives its peak value I_{Lbmax}, which can be expressed as

$$I_{Lbmax}=I_{Lbmin}+\frac{V_L}{2L_b}T_r \tag{10}$$

Meanwhile, i_r is zero at t_1, leading to ZCS-off for D_{R1} and D_{R4}. Since Q_4 is turned off at t_1, i_{Lb2} charges the intrinsic capacitor C_4 of Q_4 and discharges the intrinsic capacitor C_3 of Q_3 simultaneously. Furthermore, i_{Lb2} is I_{Lbmax} at t_1, indicating that the charge and discharge duration of C_3 and C_4 is very short

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and can be ignored. Afterward, i_{Lm} flows through Q_1 and the body diode D_3 of Q_3. As a result, both v_p and the drain-source voltage of Q_3 is zero during this mode. Both the voltages across L_{b1} and L_{b2} are $V_L - V_M$, implying both i_{Lb1} and i_{Lb2} decrease linearly and can be obtained as (11).

$$\begin{cases} i_{Lb1}(t) = i_{Lb1}(t_1) + \dfrac{V_L - V_M}{L_b}(t - t_1) \\ i_{Lb2}(t) = I_{Lbmax} + \dfrac{V_L - V_M}{L_b}(t - t_1) \end{cases} \tag{11}$$

During this mode, the discharge current path of i_{Lb1} is from ① to ② due to the initial and final values of i_{Lb1} are positive and negative, respectively. The discharge current path of i_{Lb2} is ③ due to the initial and final values of i_{Lb2} are both positive. For the LC resonant unit, i_{Lm} flows through D_3, hence, the current path of i_{Lm} and i_p is ④.

3) Mode 3 [t_2, t_3] (see Fig. 3(c)): Q_1 is turned off at t_2, and to charge the intrinsic capacitor C_1 of Q_1 and discharge the intrinsic capacitor C_2 of Q_2, i_{Lb1} should be smaller than zero at t_2. Furthermore, since the drain-source voltage of Q_3 is already zero during last mode, i_{Lb2} can charge C_1 through D_3. Consequently, the charge and discharge of C_1 and C_2 can be easily finished. Afterward, the voltages across L_{b1} and L_{b2} are V_L and $V_L - V_M$, respectively. It means that i_{Lb1} and i_{Lb2} will increase and decrease linearly, respectively. However, since both i_{Lb1} and i_{Lb2} charge C_1, the dead time, namely [t_2, t_3], can be set to be relatively small, which implies this mode can be short. Similar with Q_1 and Q_4, Q_2 and Q_3 are turned on with ZVS at t_3.

During this mode, both i_{Lb2} and i_p have the same current path as in Mode 2. And the discharge current path of i_{Lb1} is ① due to the initial and final values of i_{Lb1} are both negative.

Based on the above analysis, it can be concluded that the ZVS-on can be realized for all four switches and the ZCS can be realized for all four rectifier diodes.

III. Characteristic Analysis and Parameters Design

A. Voltage Gain and Control Method

Firstly, based on the volt-second of L_{b1} and L_{b2}, it is easy to get the relationship between V_L and V_M as

$$V_M = \frac{V_L}{1 - D_b} \tag{12}$$

Assuming the dealt power is P_o and the conversion efficiency is 100%, then the power of the primary winding should be equal to that of the secondary winding during [t_0, t_3]. Hence, the following can be obtained

$$\begin{aligned} &\int_{t_0}^{t_3} v_p(t) i_p(t)\,dt = V_M \int_{t_0}^{t_1} \left[n i_r(t) + i_m(t) \right] dt = \\ &\int_{t_0}^{t_3} n v_p(t) i_r(t)\,dt = V_H \int_{t_0}^{t_1} i_r(t)\,dt = 0.5 T_s P_o \end{aligned} \tag{13}$$

According to the symmetry of the operation principles, it is obvious that

$$\int_{t_0}^{t_1} i_m(t)\,dt = 0 \tag{14}$$

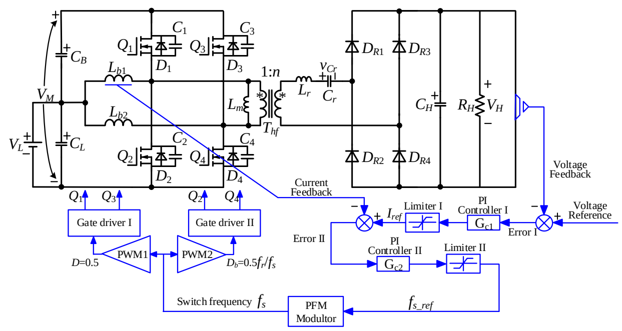

Fig. 4. Schematic of the control circuit.

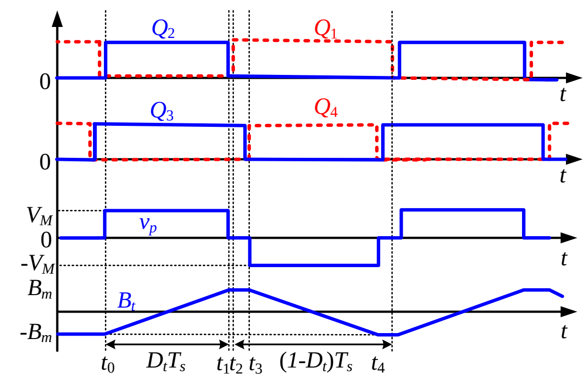

Fig. 5. Driver waveforms of the existing interleaved boost-integrated LLC converter under traditional PFM.

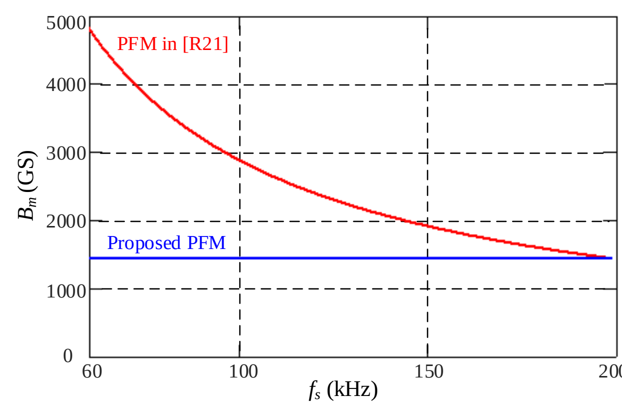

Fig. 6. The curves of B_m vs switching frequency under the two PFMs.

Referring to (12) ~ (14), it is easy to get

$$V_H = nV_M = n\frac{V_L}{1 - D_b} = n\frac{2V_L}{2 - T_r f_s} \tag{15}$$

Hence, to achieve a constant V_H, f_s can be controlled under different V_L, namely, a lower f_s under a higher V_L.

To clearly explain the control strategy, the schematic of the control circuit is drawn as Fig. 4. As can be seen, the converter adopts dual-closed-loop control, in which i_{Lb1} is the sampled value of inner current control loop and V_H is the sampled value of outer voltage control loop. At first, the error I of V_H and the reference output voltage is converted to the reference current I_{ref} of the inner control loop after the first PI controller and amplitude limiter. Subsequently, the error II of i_{Lb1} and I_{ref} is converted to the control signal after another PI controller and amplitude limiter. At last, add the control signal of

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dual-closed-loop control into the PFM modulator and transfer the appropriate f_s to the driver of the switches.

B. Resonant Capacitor C_r

When substituting (15) into (3) and (4), one can obtain

$$\begin{cases} v_{Cr}(t) = V_{Crmax}\cos\omega_r(t-t_0) \\ i_r(t) = \dfrac{V_{Crmax}}{Z_r}\sin\omega_r(t-t_0) \end{cases} \quad (t_0 \le t \le t_1) \tag{16}$$

According to (13) and (16), the following can be achieved

$$V_{Crmax} = \frac{P_o}{4 f_s V_H C_r} \tag{17}$$

To avoid the reverse resonance on the secondary side after t_1, V_{Crmax} should be smaller than V_H. Hence, C_r should satisfy with

$$C_r > \frac{P_o}{4 f_s V_H^2} \tag{18}$$

C. Boost Inductor L_b and ZVS Condition

Assuming the conversion efficiency is 100%, the power can be obtained as

$$P_o = V_L\left(I_{Lbmax} + I_{Lbmin}\right) \tag{19}$$

When substituting (10) into (19), one can obtain

$$I_{Lbmin} = \frac{P_o}{2V_L} - \frac{V_L}{4L_b}T_r \tag{20}$$

According to Fig. 2, the turn-on currents for Q_1/Q_3 and Q_2/Q_4 are $-I_{Lmmax} - i_{Lb1}(t_0)$ and $-I_{Lmmax} + I_{Lbmin}$, respectively. Obviously, the absolute value of the former is larger than that of the latter, implying the ZVS condition for Q_1/Q_3 is easier to be achieved than Q_2/Q_4. Hence, the converter ZVS condition can be derived by realizing the ZVS for Q_2/Q_4, which is

$$L_b\left(I_{Lbmin} - I_{Lmmax}\right)^2 > 2C_{oss}V_M^2 \tag{21}$$

where $C_{oss} = C_1 = C_2 = C_3 = C_4$.

According to (8), (20), and (21), the L_b can be rationally designed to be greater than 4.27 μH, and the maximum value of I_{Lbmin} is –3.13 A. The L_b used in the practical designed parameters of the prototype is 5 μH, and the value of I_{Lbmin} is –1.6 A. Hence, I_{Lbmin} is a negative value, the absolute value of the turn-on current flowing through Q_2/Q_4 will be larger. Therefore, L_{b1} and L_{b2} are designed such that their currents flow in both directions, which is more conducive to the realization of ZVS.

D. The MMFD B_m

According to the operation principles, due to the resonant capacitor voltage is always lower than the output voltage, the primary winding voltage will be clamped to zero after the normal resonance, leading to that the volt-second product of the primary winding in the half switching period is constant over the full switching frequency range. Hence, B_m is constant and can be expressed as (9), which is calculated based on the resonant frequency instead of the switching frequency. In other words, once the resonant parameters are defined, the high frequency transformer can be switching frequency-free designed.

In order to clarify the advantages of frequency-free transformer, the B_m of this paper will be compared with that of the existing interleaved boost-integrated LLC converter [21]. The driver waveforms of the existing interleaved boost-integrated LLC converter under traditional PFM are shown in Fig. 5, where the upper switch and the lower switch of each leg operate complementarily with a dead time $t_{dead} = (t_2 - t_1)$. Q_1 and Q_3 have the same duty cycle 1 - D_t but are phase-shifted with 180°, and Q_2 and Q_4 have the same duty cycle D_t but are 180° out of phase. Therefore, the conduction time of Q_2 and Q_4 is D_tT_s.

The forward resonance finishes at t_1, where the traditional MFD B_t increases from $-B_m$ to B_m. Hence, one can obtain

$$B_m = \frac{V_M}{2N_pA_e}D_tT_s \tag{22}$$

D_t can also be 0.5 at the lowest frequency f_{s_min} for the control in [21]. Hence, the traditional MMFD can be expressed as

$$B_m = \frac{V_M}{4N_p f_{s\_min} A_e} \tag{23}$$

Obviously, it is related with the switching frequency. The comparison between the above two conditions can be conducted based on the same transformer or the same MMFD.

In the case of using the same transformer, according to (9) and (23), the curves of B_m vs f_s under the two PFMs are shown in Fig. 6 (Based on the same experimental parameters in Table III). As can be seen, B_m of this paper is much lower under the same switching frequency range.

E. Comparison

As illustrated in Table I, the comparison is conducted with the other three solutions. The main disadvantage of the traditional full-bridge LLC converter is wide switching frequency range, leading to that it is difficult to design and optimize the magnetic components when the input voltage range is wide [3]. In [15], the number of semiconductors is high, which will increase the losses and cost. In [21], the adaptive frequency control is adopted, which narrows the switching frequency range but increases the complexity of the control algorithm. Most importantly, the B_m of the previous compared converters are all frequency dependent. As for the proposed converter, the input voltage range is wide and the voltage gain is independent of the load. In addition, the proposed converter does not need to adopt auxiliary inductor to achieve ZVS, and the ZVS analysis and magnetic component design are simpler. The B_m of the transformer is independent of the switching frequency, under the same parameters, which can effectively reduce the volume of the transformer.

F. Peak Currents for Switches and Diodes

According to the symmetry, Q_1 and Q_3 have the same current stress, and Q_2 and Q_4 also have the same current stress. Similarly, D_{R1} ~ D_{R4} all have the same current stress. Hence, only the peak currents of Q_1, Q_4, and D_{R1} need to be analyzed, respectively.

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TABLE I
COMPARISON WITH OTHER RESONANT CONVERTER TOPOLOGIES

Topologies	Traditional full-bridge LLC converter [3]	Interleaved boost integrated full-bridge LLC converter-I [15]	Interleaved boost integrated full-bridge LLC converter-II [21]	Proposed converter
Number of switches	4	6	4	4
Number of diodes	4	6	4	4
Auxiliary inductor for ZVS	Needed	Needed	Not needed	Not needed
Analysis of ZVS	Simple	Complex	Simple	Simple
Voltage and current stress	High	Middle	Small	Small
Soft switching	Primary switches: ZVS Secondary diodes: ZCS	Boost stage: hard-switching LLC stage: ZVS, ZCS	Primary switches: ZVS Secondary diodes: ZCS	Primary switches: ZVS Secondary diodes: ZCS
Modulation	PFM	Boost stage: PWM LLC stage: PFM	PWM/PFM	PFM
Switching frequency range	Wide	Wide	Middle	Wide
Efficiency	94%	95.4%	96%	>95.5%
Output power	576 W	1 kW	600 W	500 W
Input/output voltages	Input: 300 – 400 V Output: 48 V	Input: 110 V 60 Hz Output: 320 - 420 V	Input: 27 – 54 V Output: 360 V	Input: 37 – 62 V Output: 350 V
Switching frequency range	67 - 86.5 kHz	Boost stage: 100 kHz LLC stage: 172.3 - 208.3 kHz	100 - 200 kHz	60 - 200 kHz
Gain range	Wide	Wide	Wide	Wide
Correlation between transformer MFD and switching frequency	Dependent	Dependent	Dependent	Independent
B_m under the same transformer	High	High	Middle	Low

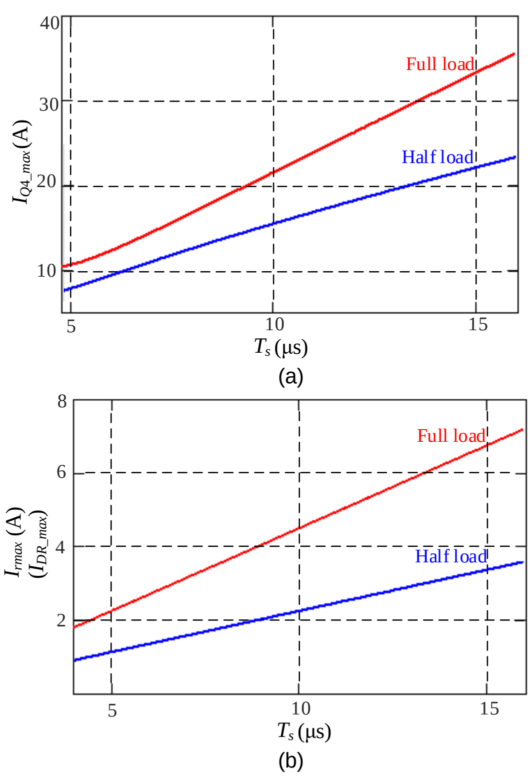

Fig. 7. Curves of the peak currents of switches and diodes under different T_s at half load and full load. (a) Peak current of switches. (b) Peak current of diodes.

In Mode 1 [t_0, t_1] (see Fig. 3(a)), i_{Lb1} decays linearly while i_{Lb2} increases linearly from I_{Lbmin}. According to the volt-second product of L_{b2}, one can obtain

$$L_b(I_{Lbmax}-I_{Lbmin})=V_L\frac{T_r}{2} \tag{24}$$

At t_3, i_{Lb1} decreases linearly to I_{Lbmin}, the voltages across L_{b1} and L_{b2} are V_L and $V_L - V_M$, respectively. Defining i_{Lb2} at t_3 as I_{Lb2_t3}, based on the volt-second product of L_{b2} from t_1 to t_3, one can obtain

$$L_{b2}(I_{Lbmax}-I_{Lb2\_t3})=(V_M-V_L)\frac{(T_s-T_r)}{2} \tag{25}$$

And at t_3, the total input current I_{in} is the sum of I_{Lb1} and I_{Lb2}, when the capacitor currents are ignored, and I_{Lb2_t3} can also be expressed as

$$I_{Lb2\_t3}=\frac{P_{in}}{V_L}-I_{Lbmin} \tag{26}$$

According to (24), (25) and (26), the following can be achieved

$$I_{Lbmin}(T_s)=\frac{P_{in}}{V_L}+\frac{(V_M-V_L)(T_s-T_r)-V_LT_r}{2L_b} \tag{27}$$

For the maximum primary current I_{pmax}, it can be expressed as

$$I_{pmax}=I_{Lmmax}+nI_{rmax} \tag{28}$$

According to the operation principles analysis in Section II, the peak current stress of Q_1 and Q_4 can be expressed as

$$i_{Q1}(T_s)\geq i_{p\_max}(T_s)-[0.5(I_{Lb\_max}(T_s)+I_{Lb\_min}(T_s))] \tag{29}$$

$$\begin{aligned}i_{Q4}(T_s)\geq\ & i_{Lm\_max}(T_s)+5i_{r\_max}(T_s)\\ &+[0.5(I_{Lb\_max}(T_s)+I_{Lb\_min}(T_s))]\end{aligned} \tag{30}$$

According to (29) and (30), I_{Q4_max} is higher than I_{Q1_max}, hence, the peak current of switches can be regard as I_{Q4_max}.

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TABLE II
PEAK CURRENTS FOR SWITCHES AND DIODES

Case	Load / Input Values	Half load (250 W)	Full load (500 W)
Switches	32 V	7.91 A	15.05 A
	53 V	10.54 A	16.25 A
	62 V	24.18 A	28.39 A
Diodes	32 V	1.12 A	2.24 A
	53 V	1.49 A	2.98 A
	62 V	3.74 A	7.48 A

TABLE III
EXPERIMENT PARAMETERS

Designed parameters	Value
Input voltage (V_L)	37-62 V
Intermediate voltage (V_M)	70 V
Output voltage (V_H)	350 V
Input capacitor (C_L)	100 µF
Intermediate capacitor (C_B)	47 µF
Rated power (P_o)	~500 W
Turns ratio (n)	5
Magnetizing inductors (L_m)	22.4 µH
Boost inductors (L_{b1} and L_{b2})	5 µH
Resonant inductor (L_r)	9 µH
Resonant capacitor (C_r)	66 nF
Output capacitor (C_H)	40 µF
Switching frequency (f_s)	60 - 200 kHz

According to (16) and (17), one can obtain

$$i_r(t) = \frac{P_o}{4 f_s V_H C_r Z_r} \sin \omega_r (t - t_0) \quad (t_0 \le t \le t_1) \tag{31}$$

Obviously, the peak current of four diodes I_{DR_max} is the peak current of I_{rmax}.

In summary, to clearly explain the peak currents of switches and diodes, , the curves of the peak currents of switches and diodes under different T_s at half load and full load are drawn in Fig. 7 according to (30) and (31) (Based on the experimental parameters in Table III). With Fig. 7 and (15), the peak currents for switches and diodes at different input voltages and loads are listed in Table II.

IV. EXPERIMENTAL RESULTS

To verify the above analysis, an experimental prototype, as shown in Fig. 8, is built. The detailed specifications of the prototype are listed in Table III, where the switching frequency range is wide from 60 kHz to 200 kHz.

According to (15), the theoretical input voltage V_L is from 35 V to 59.5 V. In the prototype, even though the actual winding turns ratio of transformer is five, the voltage ratio of secondary to primary is slightly lower than five for the existence of the leakage energy. The dead time t_d is set, which is 5% of the switching period time. Hence, the practical relationship between f_s and V_L can be expressed as

$$f_s = \frac{V_M - V_L}{0.5(1 - \frac{t_d}{T_s}) T_r V_M} \tag{32}$$

As a result, the practical V_L is from 37 V to 62 V and the relationship between f_s and V_L is shown in Fig. 9.

Referring to Fig. 6, once the same transformer is adopted both for the proposed PFM of this paper and the existing PFM

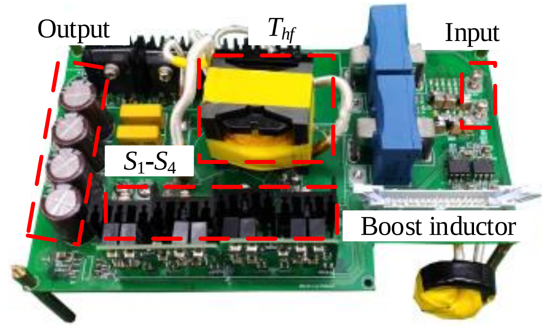

Fig. 8. Experimental prototype.

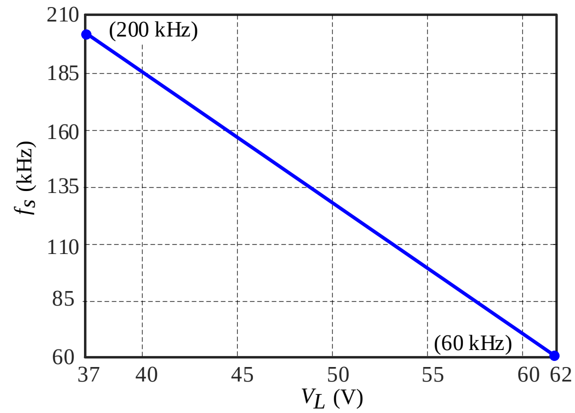

Fig. 9. Relationship between f_s and V_L.

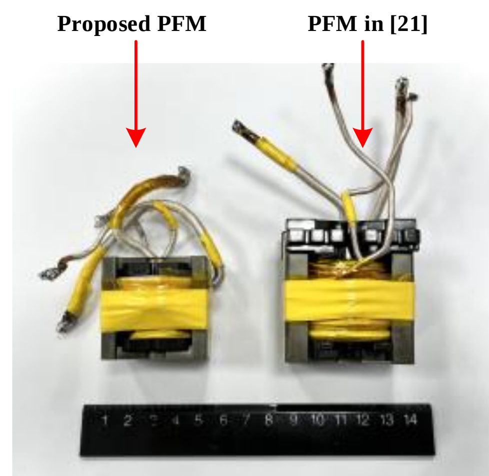

Fig. 10. Photograph of transformers under the two PFMs.

in [21], B_m of this paper can be much lower. And to further reveal the advantage of the proposed PFM, the comparison can be conducted based on the same B_m. If the same B_m is defined, the transformers for proposed PFM and the traditional PFM are made as shown in Fig. 10. As can be seen, the volume of the transformer can be decreased with the proposed PFM.

Referring to Fig. 9, to get a constant V_H, the switching frequency will decrease with the increase of the input voltage. The experimental waveforms of V_H, v_p, i_p, and i_r are shown in Fig. 11. Without loss of generality, V_H can be dual-closed-loop controlled as 350 V with three different switching frequencies under three different input voltages. It is worth noting that the positive period of v_p, i_p, and i_r keeps at a constant value of 2.5 µs under different switching frequencies. Consequently, the high frequency transformer can be designed regardless of the wide

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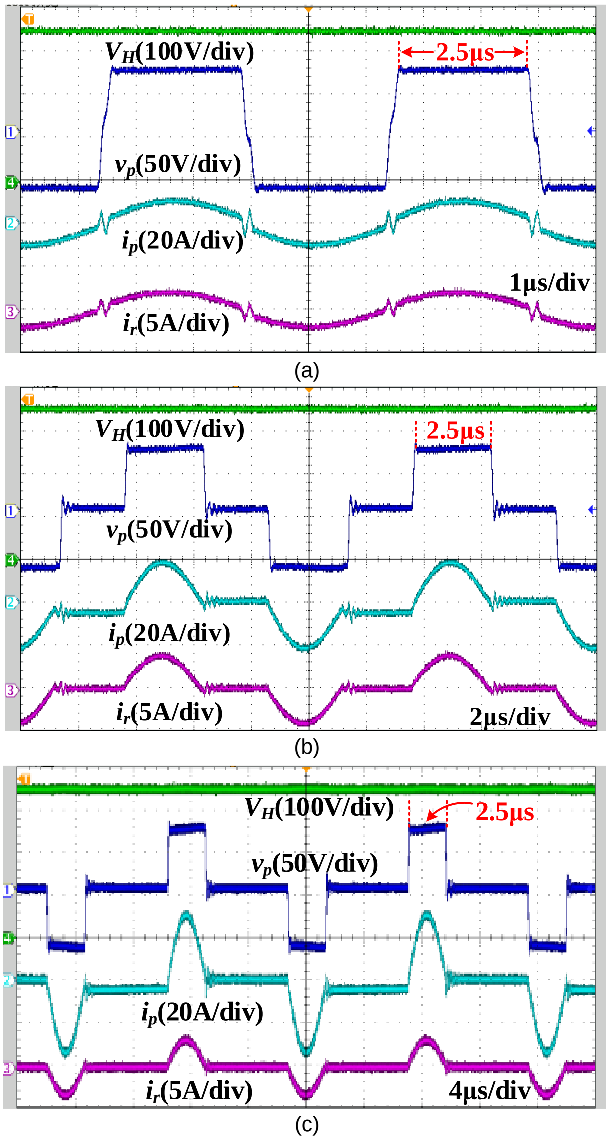

Fig. 11. Full load experimental waveforms of V_H, v_p, i_p, and i_r under different switching frequencies. (a) V_L = 37 V, f_s = 200 kHz. (b) V_L = 53 V, f_s = 100 kHz. (c) V_L = 62 V, f_s = 60 kHz.

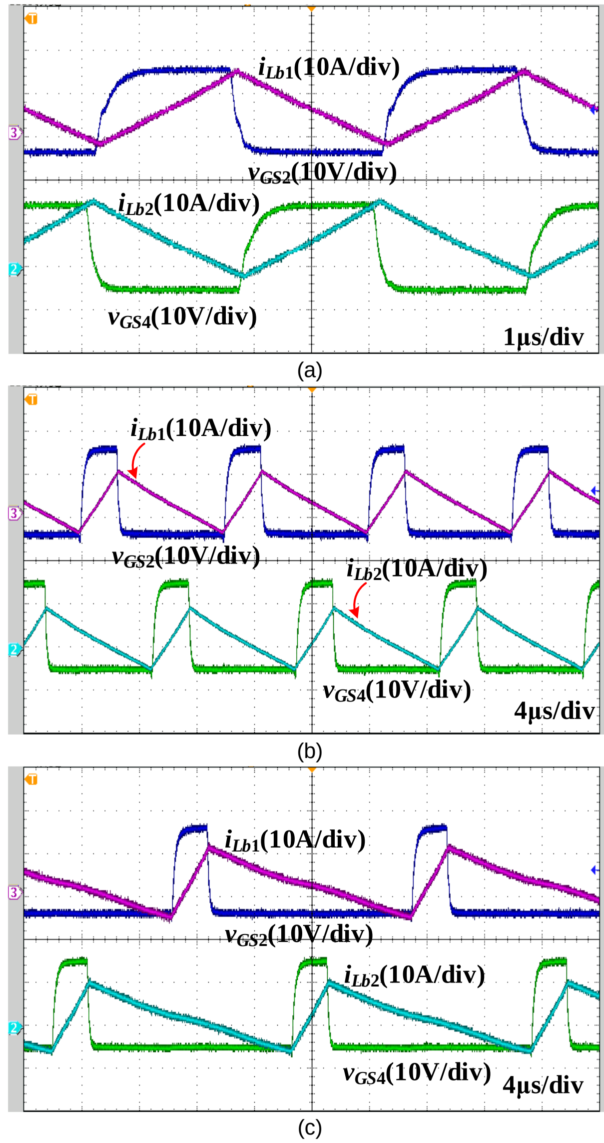

Fig. 12. Full load experimental waveforms of i_{Lb1} and i_{Lb2} under different switching frequencies. (a) V_L = 37 V, f_s = 200 kHz. (b) V_L = 53 V, f_s = 100 kHz. (c) V_L = 62 V, f_s = 60 kHz.

switching frequency range. As shown in Fig. 11(b) and (c), the currents before and after the normal resonance are different in i_p due to the existence of L_m, while they are both zero in i_r. This phenomenon is not obvious in Fig. 11(a) due to the fact that the switching frequency is close to the resonant frequency. Furthermore, the unexpected damped oscillations after the normal resonance is caused by the parasitic capacitance of the rectifier diodes, which will be detailed presented will in the following.

As can be seen from Fig. 12, i_{Lb1} and i_{Lb2} have a same shape with a half switching period phase-shift under different switching frequencies. When Q_2 (Q_4) is on, i_{Lb1} (i_{Lb2}) increases linearly, otherwise i_{Lb1} (i_{Lb2}) decays linearly. Since the output power and voltage are regulated constant, the average current of i_{Lb1} and i_{Lb2} deceases with the input voltage, and vice versa.

The ZVS waveforms for switches are shown in Fig. 13. As illustrated, ZVS can be achieved by all switches under different switching frequencies. Furthermore, the drain-source voltage of Q_1 (Q_3) has already been zero for a long enough period before it is turned on, which is more obvious under low switching frequency as shown in Fig. 13(c). Hence, the ZVS realization for Q_1 (Q_3) is easier than Q_2 (Q_4), indicating that the experimental waveforms are consistent with the theoretical analysis.

The ZCS realization for the rectifier diodes under different switching frequencies are shown in Fig. 14. As mentioned before, some unexpected oscillations occurred after the normal resonance. And apparently, there are some high frequency oscillations during the transition between D_{R1} and D_{R2}. In the prototype, the diode type is IDWD40G120C5 with output capacitance C_{oss_DR} of 90 pF. It will resonate with L_r, where the resonant capacitor 66 nF can be ignored when compared with 90 pF. And the theoretical resonant period of them is 178.8 ns. Without loss of generality, the zoomed-in waveforms of Fig. 14(b) is shown in Fig. 15. It can be found that the observed period time of the high frequency oscillation of V_{DR1} and V_{DR2} is

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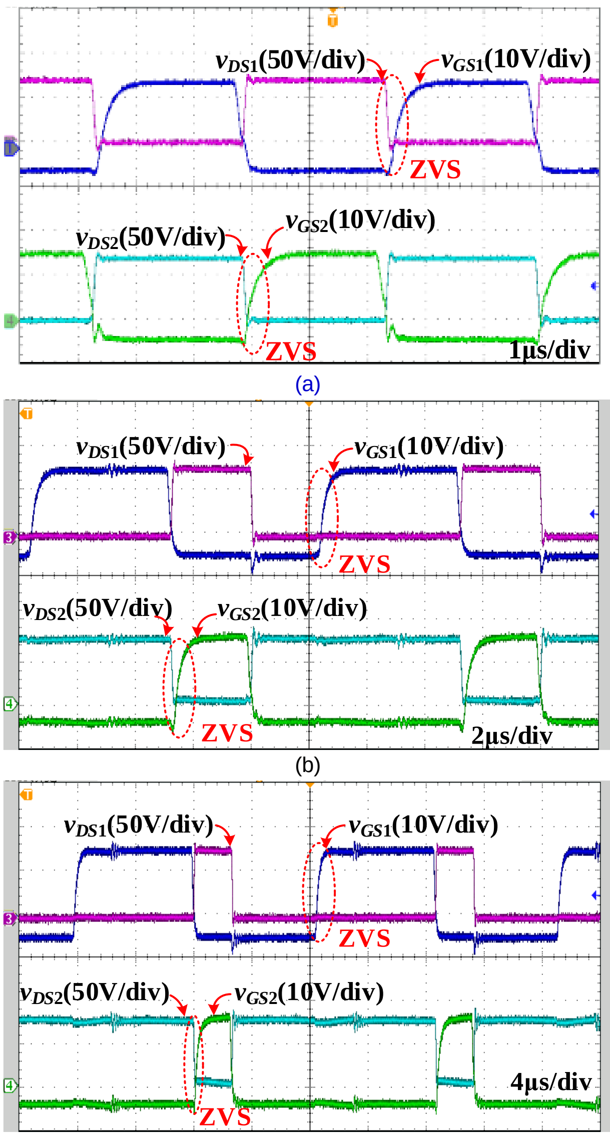

Fig. 13. Full load experimental waveforms of ZVS realization for switches under different switching frequencies. (a) V_L = 37 V, f_s = 200 kHz. (b) V_L = 53 V, f_s = 100 kHz. (c) V_L = 62 V, f_s = 60 kHz.

about 176 ns, which is close to the theoretical value. Therefore, the high frequency oscillation of V_{DR1} and V_{DR2} is caused by the resonance of the diode parasitic capacitors and the resonant inductor. Though, it should be noted that such oscillations will not affect the voltage stress of the rectifier diodes.

As shown in Fig. 16(a), no matter the output power varies from 500 W to 250 W or from 250 W to 500 W, V_H and V_M can be controlled as constant of 350 V and 70 V, respectively. Referring to Fig. 16(b), V_H and V_M can be controlled as constant as well when the input voltage changes from 44 V to 37 V.

The waveforms of input current at different switching frequencies under full load is shown in Fig. 17. As can be seen, the current ripple increases with the decrease of switching frequency. It is practically inevitable that the voltages on C_L and C_B fluctuate in a small range no matter how large C_L and C_B are designed. It is easy to know that the input current $I_{in} = P_{in}/V_L$, and the power P_{in} is constant for the output voltage V_H remains unchanged under dual-closed-loop control, therefore, the input

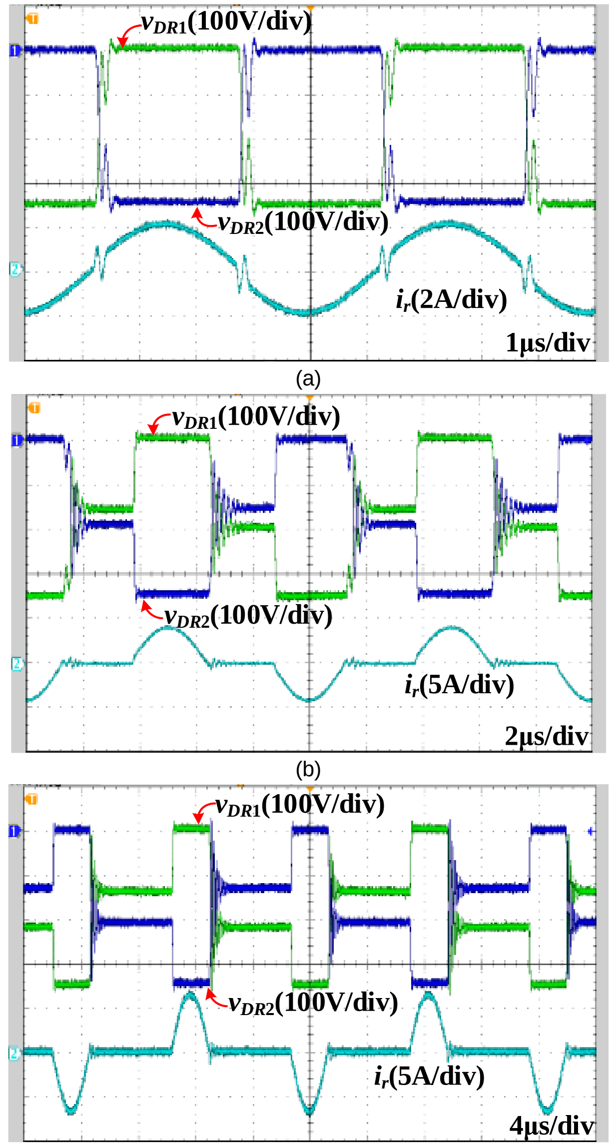

Fig. 14. Full load experimental waveforms of ZCS realization for diodes under different switching frequencies. (a) V_L = 37 V, f_s = 200 kHz. (b) V_L = 53 V, f_s = 100 kHz. (c) V_L = 62 V, f_s = 60 kHz.

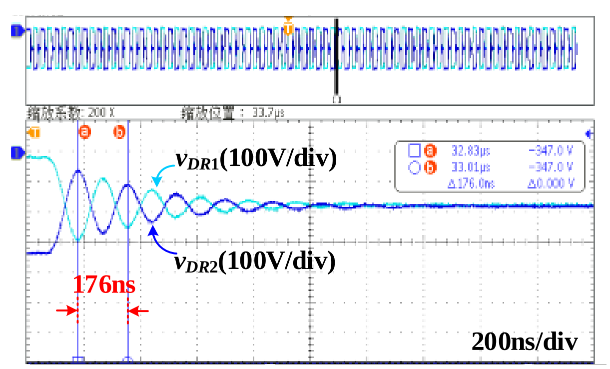

Fig. 15. Zoomed-in waveforms of Fig. 14(b).

current fluctuates with the voltage ripple of C_L. In addition, the voltage ripple becomes larger with the decrease of switching frequency due to the charge and/or discharge time of C_L becomes longer accordingly. And the lager voltage ripple causes larger input current ripple.

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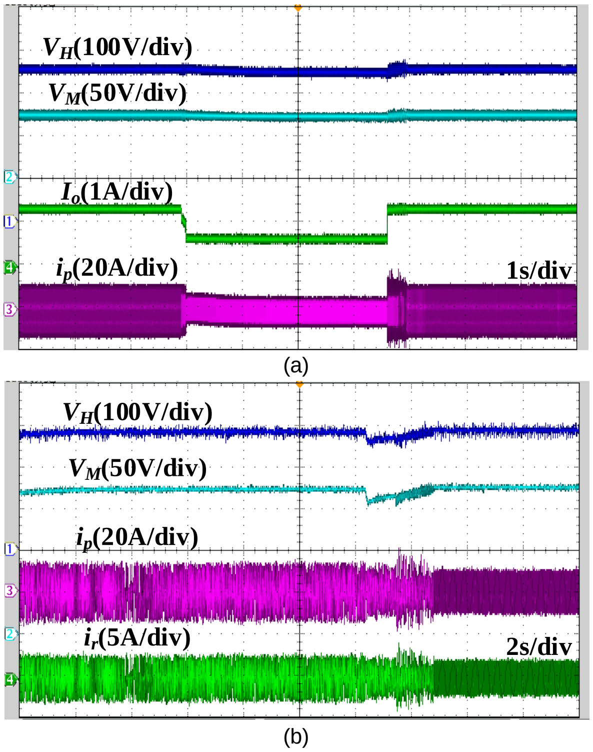

Fig. 16. Dynamic experimental waveforms. (a) Under load sudden change from 500 W to 250 W and back to 500 W. (b) Under input voltage sudden change from 44 V to 37 V.

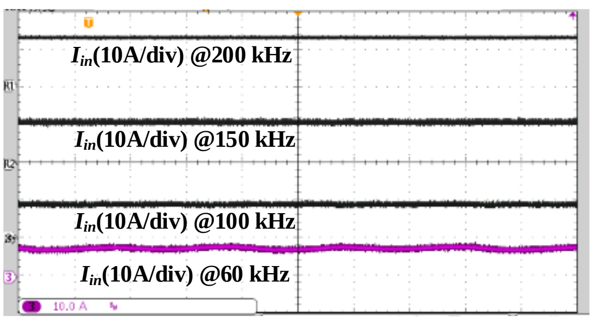

Fig. 17. The waveforms of input current at different switching frequencies under full load.

The theoretical losses under different input voltages and loads are listed in Tables IV and V, and the histogram of theoretical losses are shown in Fig. 18. As can be seen, the turn off losses and boost inductor core losses are the main losses of converter for the primary side switches cannot achieve ZVS-off and the interleaved boost unit uses two boost inductors. Driving losses, transformer copper losses and boost inductor copper losses account for a small proportion due to the total gate charge Q_g and the winding resistances of both transformer and inductor are small. Firstly, when the power is constant, with the increase of switching frequency, the main losses increase for they are all positively correlated with switching frequency while the conduction losses decrease for the RMS current values of primary switches all decrease. Secondly, when the switching frequency is constant, with the increase of power, the main losses increase while the driving losses and transformer core losses are constant for they are only related to switching frequency and independent of power.

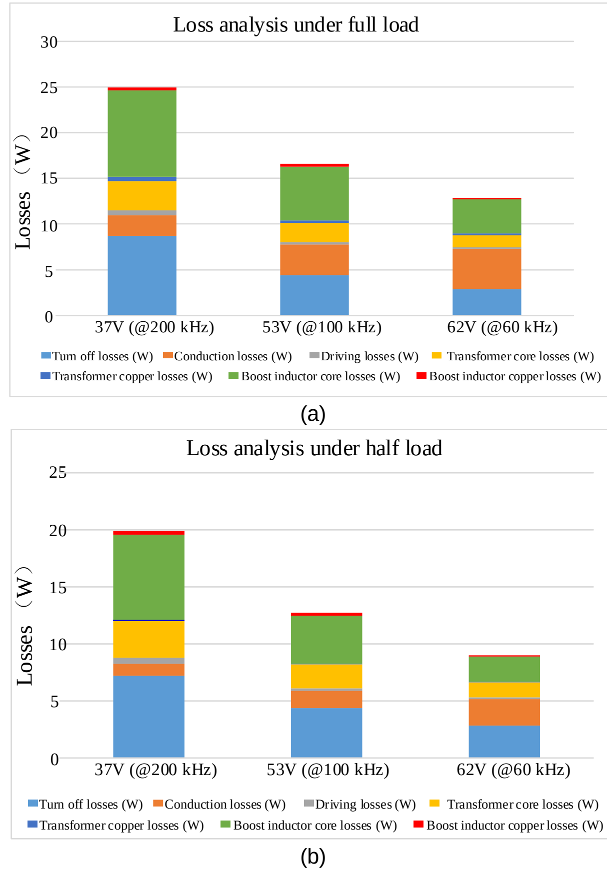

Fig. 18. Theoretical loss calculation results. (a) Full load. (b) Half load.

TABLE IV
LOSSES OF DIFFERENT INPUT VOLTAGES UNDER FULL LOAD (500 W)

Losses (W)	37V (@200 kHz)	53V (@100 kHz)	62V (@60 kHz)
Turn off losses	8.729	4.702	3.126
Conduction losses	2.268	3.36	4.43
Driving losses	0.503	0.252	0.151
Transformer core losses	3.208	2.103	1.314
Transformer copper losses	0.453	0.251	0.231
Boost inductor core losses	9.453	5.923	3.747
Boost inductor copper losses	0.342	0.282	0.154
Total losses	24.956	16.873	13.153

TABLE V
LOSSES OF DIFFERENT INPUT VOLTAGES UNDER HALF LOAD (250 W)

Losses (W)	37V (@200 kHz)	53V (@100 kHz)	62V (@60 kHz)
Turn off losses	7.244	4.402	2.886
Conduction losses	1.058	1.485	2.274
Driving losses	0.503	0.252	0.151
Transformer core losses	3.208	2.103	1.314
Transformer copper losses	0.097	0.063	0.059
Boost inductor core losses	7.486	4.206	2.203
Boost inductor copper losses	0.302	0.231	0.106
Total losses	19.898	12.742	8.993

The measured efficiency curves of different power and switching frequencies are shown in Fig. 19. When the load is constant, with the increase of switching frequency, all losses increase except for the conduction losses. Hence, the efficiency

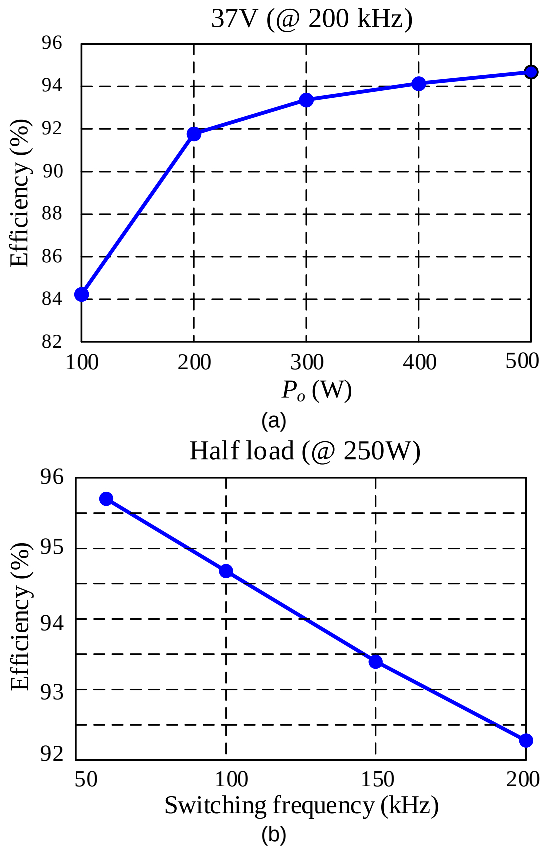

Fig. 19. Measured efficiency curves. (a) Under the same switching frequency. (b) Under the same power.

decreases with the increase of the switching frequency. While when the switching frequency is constant, with the decrease of the power, the switching and conduction losses will also decrease. Due to the B_m is a constant value, the transformer core losses are independent of the power under the same frequency, and the transformer core losses remain almost a constant value. Hence, the proportion of losses increases, and the efficiency will decrease with the decrease of the power.

V. Conclusion

With the series resonant tank is located on the secondary side, a novel interleaved boost-integrated LC series resonant converter is proposed. With the proposed pulse frequency modulation, the voltage gain of the proposed converter is only related with the interleaved boost unit under different switching frequencies since the LC series resonant unit has a fixed voltage gain. Furthermore, once the resonant parameters are defined, the MMFD of the transformer core is defined and can be kept as constant under any conditions. As a result, the high frequency transformer can be designed regardless of the wide switching frequency range. The boost inductors can be optimized to help realize the ZVS turn-on for all switches. All the theoretical analyses are verified by the experimental waveforms from 60 kHz to 200 kHz.

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