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Design Considerations for PPS Controlled Current-Fed DAB Converter to Achieve Full Load Range ZVS and Low Inductor Current Stress

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***Abstract*—Current-fed dual active bridge dc-dc converters are suited for renewable energy systems such as solar photovoltaic and fuel cells, due to the advantages of small input current ripple and wide input voltage range. In this paper, a current-fed dual active bridge dc-dc converter based on pulse width modulation plus phase shift (PPS) control is studied. The working principle and zero-voltage switching (ZVS) conditions of the converter are analyzed in depth, and it is proved mathematically for the first time that all switches can naturally achieve zero-voltage-switching (ZVS) independently of DC inductance and leakage inductance under wide input voltage range within full load range. Based on maximum power transfer, peak current and root mean square (RMS) current analysis, optimal DC inductance and leakage inductance design to obtain low inductor RMS current is proposed. In addition, the detailed loss breakdown was implemented by comparing with the non-optimized case. The effectiveness of the theoretical analysis and design method have been verified by experimental results.**

***Index Terms*—current-fed DAB, PPS Control, soft-switching analysis, parameter optimization design**

I. INTRODUCTION

Power electronic converters with bidirectional power transmission acts as a power link between low-voltage power generation side and the high-voltage bus. Dual active bridge (DAB) DC-DC converter has been widely applied to medium and high power applications duo to its advantages such as simple and symmetrical topology, bidirectional power flow, soft-switching, and so on [1], [2]. The typical voltage-fed dual active bridge (VF-DAB) consists of two active full bridge and one high-frequency transformer. The performance of the VF-DAB converter can be improved by modulation strategies improvements, such as single phase shift (SPS) [3], [4], extended phase shift (EPS) [5], dual phase shift (DPS) [6], triple phase shift (TPS) [7], etc. However, the number of working modes increases significantly when the degree of freedom increases, which could make the modulation and controller design more complex. In fact, when the voltages on both sides of the transformer do not match, the RMS current of leakage inductor in the power transmission stage will be increased. In addition, the input current ripple of VF-DAB is relatively large. This may reduce the lifetime of batteries [8]. Compared to conventional VF-DAB, CF-DAB is a good alternative for electric vehicles owing to lower input current ripples [9]. And due to the boost structure on the low voltage side, CF-DAB can operate effectively to achieve low current stress and wide ZVS range over a wide input voltage range as required by the energy storage [10]. In addition, CF-DAB is meritorious owing to inherent short circuit protection, lower high-frequency (HF) transformer turn ratio, high step-up ratio, and easier current controllability [11] – [13]. In order to adapt to wide input voltage range and reduce the current fluctuations, the current-fed dual active bridge (CF-DAB) converter is a preferred choice for low-voltage high-current systems [9] - [22].

Various control strategies have been proposed for CF-DAB converters. Using only single phase shift (SPS) control, CF-DAB can reduce current ripple significantly by interleaving structure [17]. For wide voltage variation applications, pulse width modulation plus phase shift (PPS) control can be adopted to obtain voltage matching, gaining low root mean square (RMS) current and wide zero-voltage switching (ZVS) range [18]. To further reduce circulation losses, pulse width modulation plus dual phase shift (PDPS) control [19], [20] and dual pulse width modulation plus phase shift (DPPS) control [21], [22] are proposed. Basically, these controls utilize more control degree of freedoms to obtain better performance, while, the modulations become complex. Compared with PDSP or DPPS control, PPS control is simple and easy to implement.

For PPS control, besides the PWM modulation, the implementation of soft-switching is another hot research issue because it can significantly improve the efficiency of the converter. The basic working principle and general ZVS operation are analyzed in CF-DAB under PPS control [18]. However, detail mathematical ZVS analysis and parameter

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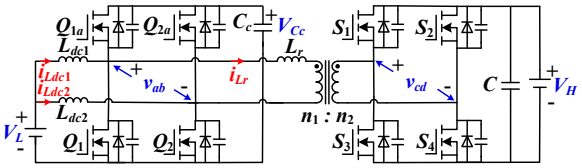

Fig.1. The topology of CF-DAB.

design are not studied. For example, the ZVS conditions for all switches are only given by the basic currents limits, and no detailed mathematic expressions are presented [18]. Furthermore, about the soft-switching analysis method, [23] - [26] give the ZVS condition, and use the graphical plots to get the region that can realize the ZVS. However, the ZVS mathematical proof remains to be studied. For example, the graphic plots are based on particular knowing specifications, which could be regarded as a "case study". Actually it is not certain what will be the ZVS performance if the application specifications are changed. In addition, when analyzing the wide voltage range or full load range performance, only some voltage points or load points are plotted to determine the region, which could also be regarded as a "case study". But there is no specific mathematical proof of whether ZVS can be realized with the full load range.

In addition, the choice of inductance is of great significance to the realization of soft-switching, power transmission and power loss. In some modulation strategies such as PDPS, the soft-switching conditions of primary and second switches are used for the selection of DC inductance and leakage inductance to ensure all switches can achieve ZVS with full load range [22], [27], [28]. However, RMS current and peak current of leakage inductor are not considered. It is important that the RMS current is related to conduction losses. [29] believes that the smaller leakage inductance leads to better performance, if ignoring the start-up current and control accuracy. In fact, this conclusion is based on a particular modulation strategy, and the characteristics of RMS current of leakage inductor are uncertain if the control strategy is changed. Besides, in order to further reduce the input current ripple, the DC inductance can be determined by current ripple in [30]. However, it does not consider the RMS current of the DC inductor. Because the design of DC and leakage inductance are seldom discussed under PPS control, the relationship between DC inductance, leakage inductance and RMS current remains to be studied, respectively.

In this paper, the ZVS performance and optimized inductance design of the CF-DAB converter under PPS control have been studied in detail. The analysis and design mainly has the following advantages.

1) The ZVS conditions for all switches are derived, and mathematically prove of nature ZVS performance regardless of power, inductance values and voltage, are given for CF-DAB under voltage matching condition. Different from previous studies, according to the instantaneous value of the inductor current, detailed mathematical expression of ZVS is obtained. In addition, it is proved mathematically for the first time that the ZVS of all switches can be achieved naturally under wide

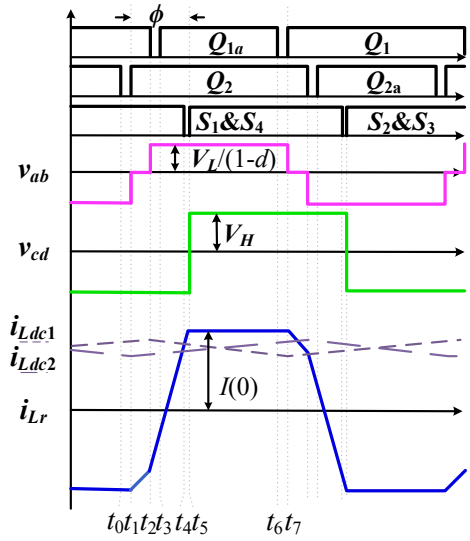

Fig.2. Steady-state waveforms of PPS for CF-DAB in boost mode. (interval A: $\phi \in [(2d\text{-}1)\,\pi, \pi]$).

input voltage range within full load range. It should be noted that the study proves that the achievement of the soft-switching is independent of any parameters, including DC inductance, leakage inductance, load power and other component parameters, when the voltage matching control is realized.

2) Parameter design for low inductor current stress is introduced. Unlike the previous studies, the maximum power transfer capability, peak current and RMS current are all considered for the inductance design. And different from other control strategies, at the wide input voltage range, the study found that the design of DC and leakage inductance need to consider the trade-off of RMS current.

3) The loss breakdown comparisons between the non-optimized case and optimized design have been analyzed at both light load and full load. And compared with the non-optimized case, the overall loss of the optimized design is reduced.

The rest of this article is organized as follows. Section II introduces the working principle of the CF-DAB converter with PPS control, and analyzes the transmission power. In section III, the ZVS conditions of all switches are analyzed in detail, and it is proved mathematically that all switches can naturally achieve ZVS under wide input voltage range with full load range. Besides, a detailed optimization design method of the inductance is given. Section IV introduces the power loss of the elements of the converter in detailed. A 650W prototype was set up in the laboratory, and the experimental results are given in Section V for verification. Finally, conclusions are drawn in Section VI.

II. Operation Principle

The topology of CF-DAB converter is depicted in Fig.1. For the low voltage side (LVS), V_L is the LVS voltage. L_{dc1} and L_{dc2} are DC boost inductors, and $L_{dc1} = L_{dc2} = L_{dc}$. If L_{dc1} and L_{dc2} have different values, the unbalanced current will occur between i_{Ldc1} and i_{Ldc2}.To achieve better current sharing

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performance, the current difference of the two inductance can be used to compensate the duty cycle of each bridge arm to balance currents. C_c is the clamping capacitor, and the voltage of the clamping capacitor is V_{Cc}. The duty ratio of the bottom switches Q_1 and Q_2 is d. The inductor L_r denotes the leakage inductance. In the high voltage side (HVS), MOSFETs S_1-S_4 form a full bridge.

Fig.2 shows the steady-state waveforms of the converter operating in boost mode when power flows from the LVS to the HVS. The wide range input voltage V_L is boosted to clamping voltage V_{Cc} to match the HVS voltage V_H by the turns of transformer. The duty cycle for the HVS switches operate 50%. And the phase-shift angle exists between the LVS and the HVS.

A. Operating Modes

The circuit mode is shown in Fig.3, and the detailed circuit analysis is as follows. And the junction capacitors of all the switches are not considered.

Stage 1 (Before t_0): During this stage, Q_1, Q_{2a}, S_2 and S_3 are turned on. v_{ab} is equal to $-V_{Cc}$, v_{cd} is equal to $-V_H$. Due to the voltage matching at this time, the leakage inductor voltage is zero, which also means that the slope of the leakage inductor current is zero. Power flows from the LVS to the HVS, and $i_{Lr} = -I(0)$.

Stage 2 (t_0-t_1): Q_{2a} is turned off at t_0. At this mode, the sum of i_{Lr} and i_{Ldc2} charges C_{2a} and discharges C_2 until the body diode of Q_2 is conducted. The condition for Q_2 to achieve ZVS conduction is $|i_{Lr}(t_0)| > i_{Ldc2}(t_0)$.

Stage 3 (t_1-t_2): At t_1, Q_2 turns on under ZVS. v_{ab} is zero, the leakage inductor current decreases in the reverse direction until Q_1 turns off. At this stage, leakage inductor voltage and the leakage inductor current can be obtained as

$$v_{Lr} = \frac{n_1 V_H}{n_2}, i_{Lr} = -I(0) + \frac{n_1 V_H}{n_2 L_r}(t - t_1) \tag{1}$$

And the duration of this stage is (2d-1) π/ω, ω is the switching angular frequency.

Stage 4 (t_2-t_3): Q_1 is turned off at t_2. The sum of $-i_{Lr}$ and i_{Ldc1} charges C_1 and discharges C_{1a} until the body diode D_{1a} of Q_{1a} is turned on. The condition for Q_{1a} to achieve ZVS conduction is $i_{Lr}(t_2) < i_{Ldc1}(t_2)$. During this mode, the voltage and current of the leakage inductor can be expressed as

$$v_{Lr} = \frac{2n_1 V_H}{n_2}, i_{Lr} = -I(0) + \frac{n_1 V_H}{n_2 L_r}\frac{(2d-1)\pi}{\omega} + \frac{2n_1 V_H}{n_2 L_r}\left(t - t_1 - \frac{(2d-1)\pi}{\omega}\right) \tag{2}$$

Stage 5 (t_3-t_4): At t_3, Q_{1a} is turned on under ZVS. The leakage inductor voltage is the same as the previous mode, so the slope of leakage current and the expression are the same. At this stage, the leakage inductor current rises to a positive value.

Stage 6 (t_4-t_5): At t_4, S_2 and S_3 are turned off. The leakage inductor current charges/discharges the junction capacitor. The condition for S_1 and S_4 to achieve ZVS is $i_{Lr}(t_4) > 0$.

Stage 7 (t_5-t_6): At t_5, S_1 and S_4 are turned on under ZVS. v_{cd} is equal to V_H. At this time, the leakage inductor voltage is zero, which also means that the slope of the leakage inductor current is zero. Power flows from the LVS to the HVS, and $i_{Lr} = I(0)$. The working mode of the second half cycle is similar to the first half cycle.

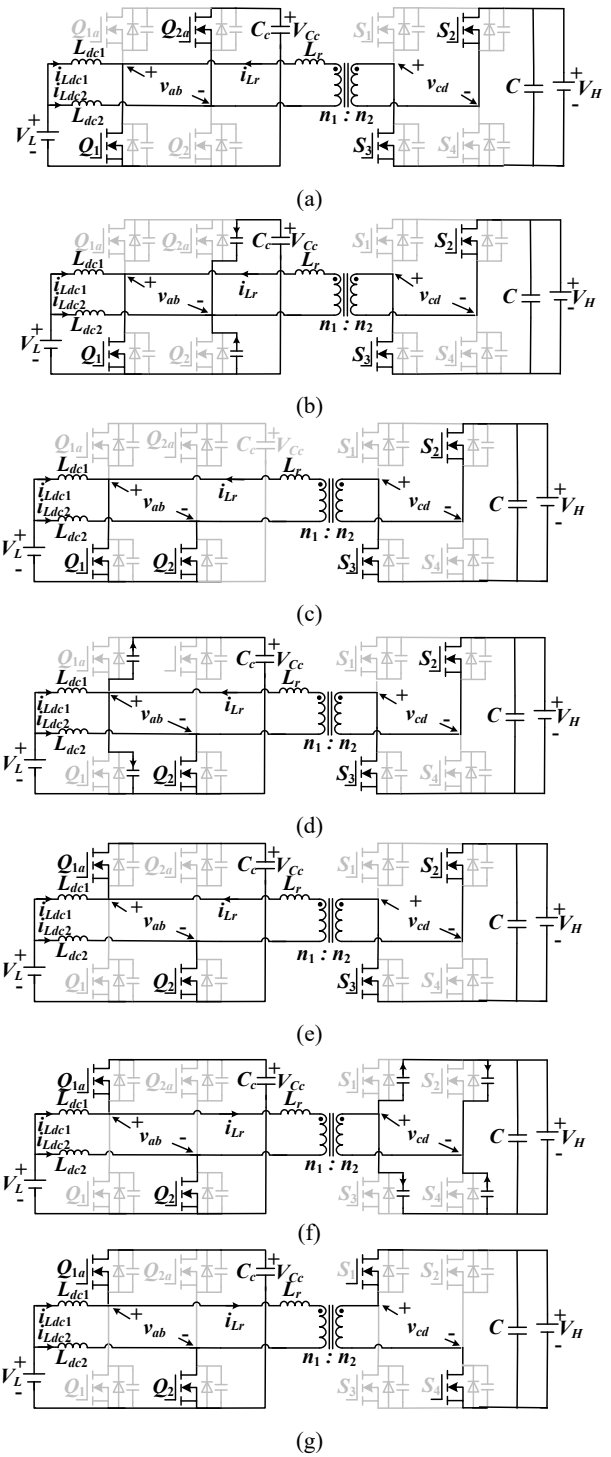

Fig.3. Operation modes of the boost mode. (a) *Before* t_0. (b) t_0-t_1. (c) t_1-t_2. (d) t_2-t_3. (e) t_3-t_4. (f) t_4-t_5. (g) t_5-t_6.

B. Power Expressions

Define that the rising edge of v_{ab} is leading v_{cd} as a positive ϕ. The total volt-seconds applied the L_{dc1} or L_{dc2} of LVS over

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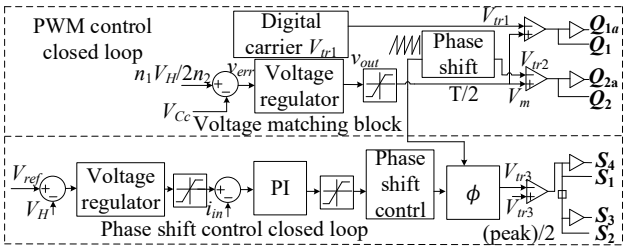

Fig.4. The diagram of the decoupling control.

one switching period are

$$V_L d + (V_L - V_{Cc})(1-d) = 0 \tag{3}$$

Then the duty cycle of Q_1 and Q_2 can be calculated as

$$d = 1 - \frac{V_L}{V_{Cc}} \tag{4}$$

PPS control strategy is realized with two individual controllers, which is the decoupling control diagram as shown in Fig.4. Voltage matching is realized strictly by voltage matching control shown in the voltage matching control block. The reference is expressed as $v_H n_1/n_2$ and the relationship between clamp voltage V_{Cc} and HVS voltage V_H in steady state is written as

$$\frac{V_{Cc}}{V_H} = \frac{n_1}{n_2} \tag{5}$$

The power can be calculated as

1) Phase shift angle $\phi \subset [0, (2d - 1)\pi]$

Based on the same method, when the phase shift angle $\phi \subset [0, (2d - 1)\pi]$, the current of leakage inductor in a whole cycle can be written as

$$-I(0) + \frac{n_1 V_H}{n_2 L_r}\frac{\phi}{2\pi}T_s - \frac{n_1 V_H}{n_2 L_r}\left(\frac{(2d-1)}{2} - \frac{\phi}{2\pi}\right)T_s = I(0) \tag{6}$$

Through integration of the transformer voltage and current, the power can be calculated as

$$P = \frac{1}{T_s}\int_0^{T_s} i_{Lr} v_{ab}\,dt = \frac{2}{T_s}\left[\int_{\frac{(2d-1)}{2}T_s}^{\frac{T_s}{2}} I(0)\frac{n_1 V_H}{n_2}\,dt\right] \tag{7}$$

Substituting (6) into (7), the output power is can be written as

$$P = \frac{(n_1 V_H)^2 (1-d)\left[\phi - (d-0.5)\pi\right]T_s}{(n_2)^2 \pi L_r} \tag{8}$$

2) Phase shift angle $\phi \subset [(2d - 1)\pi, \pi]$

According to the analyses of working modes in section II-A, the current of leakage inductor in a whole cycle can be written as

$$-I(0) + \frac{n_1 V_H}{n_2 L_r}\frac{(2d-1)}{2}T_s + \frac{2n_1 V_H}{n_2 L_r}\left(\frac{\phi}{2\pi} - \frac{(2d-1)}{2}\right)T_s = I(0) \tag{9}$$

Through integration of the transformer voltage and current, the power can be calculated as

$$P = \frac{1}{T_s}\int_0^{T_s} i_{Lr} v_{ab}\,dt = \frac{2}{T_s}\left[\int_{\frac{(2d-1)}{2}T_s}^{\frac{\phi}{2\pi}T_s}\left[-I(0) + \frac{n_1 V_H}{n_2 L_r}\frac{(2d-1)}{2}T_s + \frac{2n_1 V_H}{n_2 L_r}\left(\frac{\phi}{2\pi} - \frac{(2d-1)}{2}\right)T_s\right]\frac{n_1 V_H}{n_2}\,dt + \int_{\frac{\phi}{2\pi}T_s}^{\frac{T_s}{2}} I(0)\frac{n_1 V_H}{n_2}\,dt\right] \tag{10}$$

Substituting (9) into (10), the output power is can be written as

$$P = \frac{(n_1 V_H)^2\left[-\phi^2 + 2d\pi\phi - d(2d-1)\pi^2\right]T_s}{2(n_2)^2\pi^2 L_r} \tag{11}$$

Thus, the power can be written as

$$P = \begin{cases} \dfrac{(n_1 V_H)^2(1-d)\left[\phi - (d-0.5)\pi\right]T_s}{(n_2)^2\pi L_r} & \phi \in \left[0, (2d-1)\pi\right] \\ \dfrac{(n_1 V_H)^2\left[-\phi^2 + 2d\pi\phi - d(2d-1)\pi^2\right]T_s}{2(n_2)^2\pi^2 L_r} & \phi \in \left[(2d-1)\pi, \pi\right] \end{cases} \tag{12}$$

Fig.5 illustrates the power transfer curves under different V_L. When the voltage is matched and ϕ range is [0, 0.5π], P increases monotonically as ϕ increases.

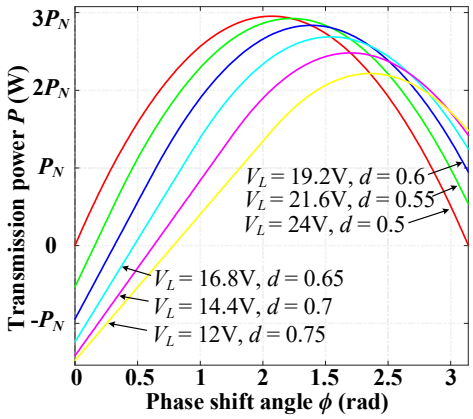

Fig.5. Curves of power and phase shift angle.

III. Soft-Switching Analysis and Optimized Design

A. ZVS Range Analysis

In this section, the conditions of ZVS for all switches are derived based on the DC inductor current and leakage inductor current. In addition, it is proved mathematically that all switches can naturally achieve ZVS at wide input voltage range within full load range. The study proves that, when the voltages are matched, the implementation of the soft-switching is independent of any parameters, including DC inductance, leakage inductance, load power and other component parameters. The analysis process is shown as follows.

In order to achieve ZVS of Q_1 and Q_2, the current limit of ZVS $I_{\_ZVS\_\ Q1\&Q2} = i_{Ldc2}(t_0) + i_{Lr}(t_0) < 0$ needs to be satisfied. Based on mode analysis and calculation of instant current value, the current at switch turn-on for charging (discharging) the junction capacitor C_{2a} (C_2) to achieve ZVS of Q_1 and Q_2 is written as

$$I_{ZVS\_Q_1\&Q_2} = i_{Ldc2}(t_0) + i_{Lr}(t_0) = \begin{cases} \dfrac{n_1 V_H d(d-1)T_s}{2n_2 L} & P \le P_{div} \\ \dfrac{P}{2V_L} + \dfrac{n_2 V_L^2 T_s}{2n_1 V_H L_{dc}} - \dfrac{V_L T_s}{2L_{dc}} - \dfrac{n_1 V_H T_s}{4n_2 L_r} + \dfrac{1}{2L_r}\sqrt{\left(\dfrac{n_1 V_H}{n_2}T_s\right)^2 d(1-d) - 2L_r P T_s} & P \ge P_{div} \end{cases} \tag{13}$$

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P_{div} is determined by (12) with $\phi = (2d - 1)\pi$. And it can be written as

$$P_{div} = -\frac{n_1^2 V_H^2 T_s \left(2d^2 - 3d + 1\right)}{2n_2^2 L_r} \tag{14}$$

The current limit of ZVS $I_{\_ZVS\_Q1a\&Q2a} = i_{Lr}(t_2) - i_{Ldc1}(t_2) < 0$ needs to be satisfied to achieve ZVS of Q_{1a} and Q_{2a}. The same method can be used to obtain the current at switch turn-on for charging (discharging) the top switching junction capacitor C_{1a} (C_1) to achieve ZVS of Q_{1a} and Q_{2a} is written as

$$I_{ZVS\_Q_{1a}\&Q_{2a}} = i_{Lr}(t_2) - i_{Ldc1}(t_2) = \begin{cases} \dfrac{n_1 V_H d(d-1) T_s}{2n_2 L} & P \le P_{div} \\ -\dfrac{P}{2V_L} + \dfrac{n_2 V_L^2 T_s}{2n_1 V_H L_{dc}} - \dfrac{V_L T_s}{2L_{dc}} - \dfrac{n_1(3-4d)V_H T_s}{4n_2 L_r} + \dfrac{1}{2L_r}\sqrt{\left(\dfrac{n_1 V_H}{n_2} T_s\right)^2 d(1-d) - 2L_r P T_s} & P \ge P_{div} \end{cases} \tag{15}$$

And the current limit of ZVS $I_{\_ZVS\_S1\&S2\&S3\&S4} = i_{Lr}(t_4) > 0$ needs to be satisfied to achieve ZVS of S_1 - S_4. The ZVS current at switch turn-on for charging (discharging) the junction capacitor of the high-voltage side full bridge switch is written as

$$I_{ZVS\_S_1\&S_2\&S_3\&S_4} = i_{Lr}(t_4) = \begin{cases} \dfrac{n_1 V_H (2d-1) T_s}{4n_2 L_r} & P \le P_{div} \\ \dfrac{\dfrac{n_1 V_H T_s}{n_2} - 2\sqrt{\dfrac{n_1 V_L V_H}{n_2} T_s^2 - 2L_r P T_s - T_s^2 V_L^2}}{4L_r} & P \ge P_{div} \end{cases} \tag{16}$$

To obtain the minimal value of (13), rewrite the above current at switch turn-on $I_{\_ZVS\_Q1\&Q2}$ into a univariate function with load power P as independent variable, and its derivative can be expressed as

$$\frac{\partial I_{ZVS\_Q_1\&Q_2}(P)}{\partial P} = \begin{cases} 0 & P \le P_{div} \\ \dfrac{1}{2V_L} - \dfrac{T_s}{2\sqrt{\left(\dfrac{n_1 V_H}{n_2} T_s\right)^2 d(1-d) - 2L_r P T_s}} & P \ge P_{div} \end{cases} \tag{17}$$

As can be seen, $I'_{\_ZVS\_Q1\&Q2}$ is equal to 0 when P is belonging to [0, P_{div}]. When P is in the region [0, P_{div}], the value of $I_{\_ZVS\_Q1\&Q2}$ is constant. When P is in the region [P_{div}, P_N], according to (4) and (5), $I'_{\_ZVS\_Q1\&Q2}$ can be written as

$$I'_{ZVS\_Q_1\&Q_2} = \frac{1}{2V_L}\left(1 - \frac{1}{\sqrt{1 - \dfrac{1}{1-d} - \dfrac{2L_r P}{V_L^2 T_s}}}\right) \tag{18}$$

Since $(1/(1\text{-}d))$ and $(2L_rP/TV_L\text{^}2)$ of above formula are both greater than zero in (18), the condition of ZVS can be further written as

$$0 < 1 - \frac{1}{1-d} - \frac{2L_r P}{V_L^2 T_s} \le 1 \tag{19}$$

According to (18) and (19), $I'_{\_ZVS\_Q1\&Q2}$ is less than zero when P is in the region [P_{div}, P_N]. Therefore, $I_{\_ZVS\_Q1\&Q2}$ is decreasing monotonically over this interval, and since $I_{\_ZVS\_Q1\&Q2}$ is continuous over the entire interval [0, P_N], this means that as long as $I_{\_ZVS\_Q1\&Q2}$ is less than zero when $P = 0$, $I_{\_ZVS\_Q1\&Q2}$ will always be smaller than zero, which means Q_1 and Q_2 can achieve ZVS in full load range. As can be seen that in (13), (d − 1) is less zero when $P \leqslant P_{div}$. Therefore, switches Q_1 and Q_2 can naturally achieve ZVS at full load range.

The same analysis is applied to the switches Q_{1a} and Q_{2a}, the derivative of current at switch turn-on $I_{\_ZVS\_Q1a\&Q2a}$ with load power P as independent variable can be obtained as

$$\frac{\partial I_{ZVS\_Q_{1a}\&Q_{2a}}(P)}{\partial P} = \begin{cases} 0 & P \le P_{div} \\ -\dfrac{1}{2V_L} - \dfrac{T_s}{2\sqrt{\left(\dfrac{n_1 V_H}{n_2} T_s\right)^2 d(1-d) - 2L_r P T_s}} & P \ge P_{div} \end{cases} \tag{20}$$

$I_{\_ZVS\_Q1a\&Q2a}$ is monotonically decreasing and continuous over the entire interval [0, P_N], so as long as $I_{\_ZVS\_Q1a\&Q2a}$ is less

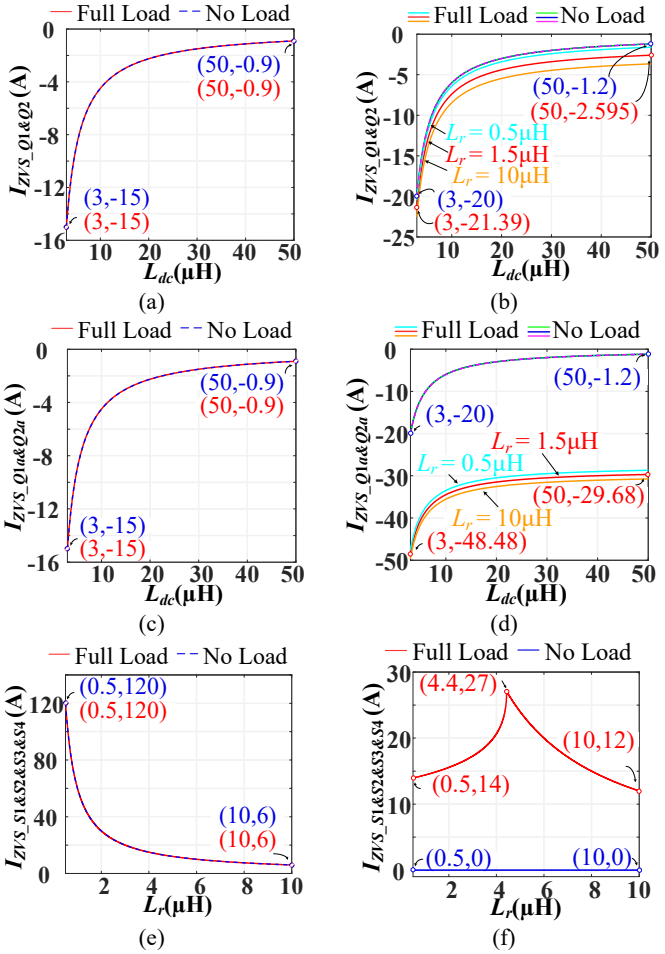

Fig.6. Current at switch turn-on. (a) Q_1&Q_2 V_L = 12V. (b) Q_1&Q_2 when V_L = 24V. (c) Q_{1a}&Q_{2a} V_L = 12V. (d) Q_{1a}&Q_{2a} when V_L = 24V. (e) S_1&S_2&S_3&S_4 when V_L = 12V. (f) S_1&S_2&S_3&S_4 when V_L = 24V. (V_L = 12 ~ 24V, V_H = 240V, P_N = 650W).

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than zero when $P = 0$, switches Q_{1a} and Q_{2a} can realize ZVS at full load range. As can be seen that in (15), $(d - 1)$ is less zero when $P \leqslant P_{div}$. Therefore, switches Q_{1a} and Q_{2a} can naturally achieve ZVS at full load range.

The same analysis is applied to the switches S_1, S_2, S_3 and S_4, the derivative of current at switch turn-on $I_{\_ZVS\_S1\&S2\&S3\&S4}$ with load power P as independent variable can be obtained as

$$\frac{\partial I_{ZVS\_S_1\&S_2\&S_3\&S_4}(P)}{\partial P} = \begin{cases} 0 & P \le P_{div} \\ \dfrac{T_s}{2\sqrt{\left(\dfrac{n_1 V_H}{n_2} T_s\right)^2 d(1-d) - 2L_r P T_s}} & P \ge P_{div} \end{cases} \tag{21}$$

$I_{\_ZVS\_S1\&S2\&S3\&S4}$ is monotonically increasing and continuous over the entire interval $[0, P_N]$, so as long as $I_{\_ZVS\_S1\&S2\&S3\&S4}$ is greater than zero or equal to zero when $P = 0$, switches S_1, S_2, S_3 and S_4 can realize ZVS at full load range. As can be seen that in (16), $(2d - 1)$ is bigger than zero when $P \leqslant P_{div}$. Therefore, switches S_1, S_2, S_3 and S_4 can naturally achieve ZVS at full load range.

To verify the theoretical proof, take the following parameters as an example: $V_L = 12 \sim 24$V, $V_H = 240$V, $f = 100$kHz, $P_N = 650$W. Fig.6 shows the current at switch turn-on. When $V_L = 12$V, P is belonging to $[0, P_{div}]$, ZVS of Q_1 and Q_2 is shown in Fig.6 (a). The current at switch turn-on $I_{\_ZVS\_Q1\&Q2} = -0.9\text{A} < 0$ with very large DC inductance $L_{dc} = 50\mu$H under no load, and the current at switch turn-on $I_{\_ZVS\_Q1\&Q2} = -15\text{A} < 0$ with very small DC inductance $L_{dc} = 3\mu$H under no load, this means that switches Q_1 and Q_2 can achieve ZVS when $V_L = 12$V under different DC inductances with no load. Meanwhile, the current at switch turn-on $I_{\_ZVS\_Q1\&Q2}$ is also less than zero at full load, which means that switches Q_1 and Q_2 can achieve ZVS when $V_L = 12$V under different DC inductances within full load range. When $V_L = 24$V, P belongs to $[P_{div}, P_N]$, ZVS of Q_1 and Q_2 is shown in Fig.6 (b). The current at switch turn-on $I_{\_ZVS\_Q1\&Q2} = -1.2\text{A} < 0$ with very large DC inductance $L_{dc} = 50\mu$H and $L_r = 1.5\mu$H under no load, and the current at switch turn-on $I_{\_ZVS\_Q1\&Q2} = -20\text{A} < 0$ with very small DC inductance $L_{dc} = 3\mu$H and $L_r = 1.5\mu$H under no load, this means that switches Q_1 and Q_2 can achieve ZVS when $V_L = 24$V under different DC inductances with no load. Meanwhile, the current at switch turn-on $I_{\_ZVS\_Q1\&Q2} = -2.595\text{A} < 0$ with very large DC inductance $L_{dc} = 50\mu$H and $L_r = 1.5\mu$H under full load, and the current at switch turn-on $I_{\_ZVS\_Q1\&Q2} = -21.39\text{A} < 0$ with very small DC inductance $L_{dc} = 3\mu$H and $L_r = 1.5\mu$H under full load, this means that switches Q_1 and Q_2 can achieve ZVS when $V_L = 24$V under different DC inductances within full load range. The current at switch turn-on $I_{\_ZVS\_Q1\&Q2}$ is less than zero not only when leakage inductance $L_r = 1.5\mu$H, but also when $L_r = 0.5\mu$H and $L_r = 10\mu$H. To sum up, Fig.6 (a) and (b) verify switches Q_1 and Q_2 can achieve ZVS under different DC and leakage inductances at full input voltage range within full load range.

For Q_{1a} and Q_{2a}, the ZVS of Q_{1a} and Q_{2a} is shown in Fig.6 (c) and Fig.6 (d). As can be seen, the same theory could verify that switches Q_{1a} and Q_{2a} can achieve ZVS under different DC and leakage inductances at full input voltage range within full load range. For S_1, S_2, S_3 and S_4, ZVS of S_1, S_2, S_3 and S_4 is shown in Fig.6 (e) and Fig.6 (f). As can be seen, since the junction capacitor is not considered, ZVS is not achieved at just one point for HVS switches, that is $V_L = 24$V, $P = 0$. In addition, the same theory could verify that switches S_1, S_2, S_3 and S_4 can achieve ZVS under different DC and leakage inductances at other input voltages and load powers.

It has been proved that any inductance parameter can make the converter realize ZVS at full input voltage range within full load range, so how to determine the value of DC and leakage inductance becomes a key problem. Therefore, in order to determine the DC and leakage inductance, the maximum power transmission capability and inductor current stress need to be analyzed.

B. DC and Leakage Inductances Optimization

In this section, the parameter considerations for DC and leakage inductances are discussed with the goals of achieving both low inductor current stress and maximum power transfer. The related parameters are: $V_L = 12 \sim 24$V, $V_H = 240$V, $P_N = 650$W. According to (4), the duty cycle range is $0.5 \sim 0.75$. In this paper, the design of converter is under the condition of rated load power. And the power loss is maximum at the rated power. As long as the converter can run safely and reliably when the maximum loss is met, the converter can run safely under different loss conditions in the full load range.

From the relationship between the transmission power and the phase shift angle ϕ in Fig.5, when the phase shift angle $\phi = 0.5\pi$, the relationship between the transmission power versus the leakage inductance and the duty cycle is written as

$$P(L_r, d) = \frac{(n_1 V_H)^2 T_s \left[-8d^2 + 8d - 1\right]}{8 n_2^2 L_r} \tag{22}$$

Fig.7 shows that the leakage inductance range for different d when the maximal power is equal to P_N. Consequently, based on Fig.7, $L_r \leq 2.215\mu$H should be satisfied to achieve maximum power transfer at the extreme case.

Under rated power P_N, the RMS current and peak current of the leakage inductor can be calculated as (23) and (24),

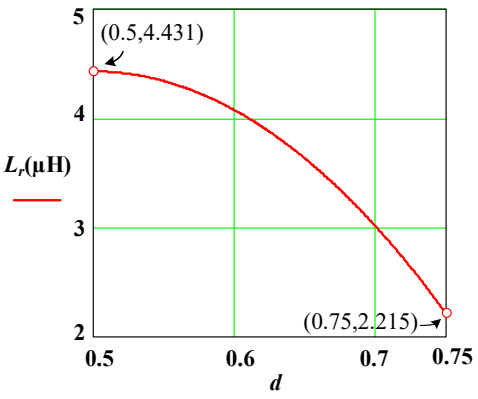

Fig.7. Relation between transmission power to leakage inductance and duty cycle. ($\phi = 0.5\pi$, $P_N = 650$W).

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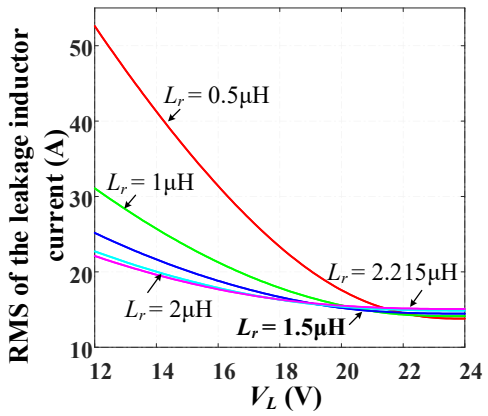
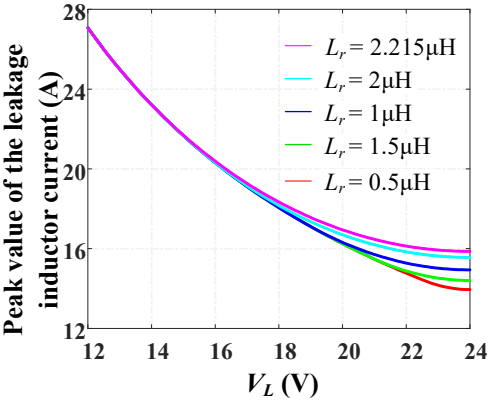
$$I_{Lr\_RMS}=\begin{cases}\dfrac{n_1V_HT_s}{2n_2\pi L_r}\sqrt{2\phi(1-d)\left[\phi-(2d-1)\pi\right]-\dfrac{\pi^2}{12}(2d-1)^2(4d-5)} & \left\{\begin{matrix}V_{L\_\min}\le V_L\le V_{L\_div}\\ \phi\in\left[0,(2d-1)\pi\right]\end{matrix}\right\}\\ \dfrac{n_1V_HT_s}{n_2\pi L_r}\sqrt{\dfrac{\phi\left[\phi(\pi d-\phi)+3\pi^2d(1-2d)\right]}{6\pi}+\dfrac{\pi^2(2d-1)^2(4d-1)}{16}} & \left\{\begin{matrix}V_{L\_div}\le V_1\le V_{L\_\max}\\ \phi\in\left[(2d-1)\pi,\pi\right]\end{matrix}\right\}\end{cases} \tag{23}$$



(a)



(b)

Fig.8. Curves for current of the leakage inductor. (a) RMS currents under different leakage inductor values. (b) peak currents under different leakage inductor values.

respectively.

$$I_{Lr\_peak}=\begin{cases}\dfrac{P}{2V_L} & \phi\in\left[0,(2d-1)\pi\right]\\ \dfrac{n_1V_HT_s}{4n_2L_r}-\dfrac{\sqrt{\dfrac{n_1V_HV_L}{n_2}T_s^2-V_L^2T_s^2-2L_rPT_s}}{2L_r} & \phi\in\left[(2d-1)\pi,\pi\right]\end{cases} \tag{24}$$

Under PPS modulation, the converter operates in two modes. Thus, the mode boundary of input voltage should be calculated. In order to determine the interval boundary of input voltage, taking $\phi = (2d - 1)\pi$ into (12), the output power with duty cycle as independent variable can be expressed as

$$P(d)=-\frac{(n_1V_H)^2\left(2d^2-3d+1\right)T_s}{(n_2)^2L_r} \tag{25}$$

Under rated power P_N, the interval boundary of duty cycle d can be calculated as

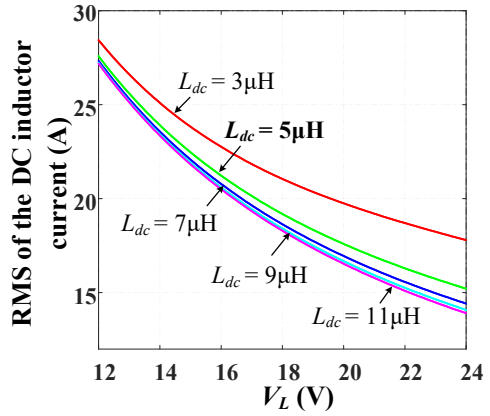


Fig.9. RMS currents under different DC inductor values.

$$d_{div}=0.75-\frac{n_2}{4n_1V_HT_s}\sqrt{\frac{T_s^2n_1^2V_H^2}{n_2^2}-16L_rP_NT_s} \tag{26}$$

Then, according to (26) and (4) in the manuscript, the interval boundary of input voltage can be written as $V_{L\_div}=V_{Cc}(1-d_{div})$.

In addition, The RMS current of the DC inductor can be calculated as

$$I_{L\_RMS}=\sqrt{\frac{P_N^2}{4V_L^2}+\frac{V_L^2T_s^2}{12L^2}\left(\frac{n_2V_L}{n_1V_H}-1\right)^2} \tag{27}$$

Fig.8 illustrates the curves for the inductor current. Fig.8 (a) and (b) illustrates the relationship between the RMS current, peak current and the input voltage for different leakage inductance, respectively. It should be noted that, unlike other control strategies, RMS current of the leakage inductor is related to the input voltage V_L. For example, when V_L is equal to 12V, smaller leakage inductance leads to larger RMS current. When V_L is equal to 24V, smaller leakage inductance leads to smaller RMS current. Besides, lower leakage inductance will lead to smaller peak current at the full input voltage range.

As can be seen, when the leakage inductance L_r is equal to 0.5μH, the RMS current increases significantly if the input voltage is low; when L_r is larger than 2μH, the leakage inductor RMS currents change slightly. Considering that more windings will be needed to increase the inductance, the leakage inductance is designed to be 1.5μH to make a tradeoff between RMS current and inductor losses.

According to the general engineering design, the DC current ripple is set in a range such as 15% - 100%, with substitution of all the parameters, the DC inductance region is about 3-11μH. Fig.9 illustrates the RMS current curves of the DC inductor. Similar to leakage inductance, considering the magnetic loss of the DC inductor and the RMS current, L_{dc} = 5μH is finally selected for the DC inductance.

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IV. Comparison of Loss

In this section, the loss breakdown comparisons between the non-optimized case and the optimized design have been analyzed at both light load and full load. The total losses consist of four parts, namely driving loss, switches loss, inductor loss, and transformer loss. The loss breakdown of each part is analyzed as follows.

A. Driving Loss

Driving loss can be calculated as

$$\begin{aligned} P_{dri\_loss} &= P_{dri\_LVS} + P_{dri\_HVS} \\ &= 4\left(V_{gs\_on} - V_{gs\_off}\right)Q_{g\_LVS}f_s + 4\left(V_{gs\_on} - V_{gs\_off}\right)Q_{g\_HVS}f_s \end{aligned} \tag{28}$$

Where the positive voltage of driving signal V_{gs_on} is 15V, the negative voltage of driving signal V_{gs_off} is −5V. Device type IPP023N10N5 from Infineon company is selected for LVS switches, and the junction capacitor of LVS switch is 1810pF. Meanwhile, device type UJ3C065030K3S from United-SiC company is selected for HVS switches, and the junction capacitor of LVS switch is 320pF.The gate charge of each LVS switch Q_{g_LVS} is 210nC, the gate charge each HVS switch Q_{g_HVS} is 50nC.

B. Switches Loss

1) *Switches conduction loss*

Conduction loss can be calculated as

$$P_{con\_loss} = P_{con\_LVS} + P_{con\_HVS} = 2\left(\frac{I_{D\_rms\_Q1a}}{\sqrt{2}}\right)^2 R_{DS\_LVS} + 2\left(\frac{I_{D\_rms\_Q2}}{\sqrt{2}}\right)^2 R_{DS\_LVS} + 4\left(\frac{I_{D\_rms\_S1}}{\sqrt{2}}\right)^2 R_{DS\_HVS} \tag{29}$$

The drain-source on-resistance is designed according to room temperature. R_{DS_LVS} = 2.3mΩ is selected for on-resistance of LVS switch. R_{DS_HVS} = 27mΩ is selected for on-resistance of HVS switch. The RMS current of drain current value of switches is given as the following.

$$\begin{cases} I_{D\_rms\_Q1a} = \sqrt{\dfrac{1}{(1-d)T_s}\left[\int_{t_3}^{t_6}\left(i_{Ldc1}(t) - i_{Lr}(t)\right)^2 dt\right]} \\ I_{D\_rms\_Q2} = \sqrt{\dfrac{1}{dT_s}\left[\int_{t_1}^{t_8}\left(i_{Ldc2}(t) + i_{Lr}(t)\right)^2 dt\right]} \\ I_{D\_rms\_S1} = \sqrt{\dfrac{2}{T_s}\left[\int_{t_5}^{t_{10}} i_{Lr}(t)^2 dt\right]} \end{cases} \tag{30}$$

2) *Switches turn-on loss*

According to the ZVS range analysis of all switches in III-A, the converter can achieve full load range ZVS with full input voltage range for all switches. Therefore, the switches turn-on loss can be considered as

$$P_{turn-on\_loss} = 0 \tag{31}$$

3) *Switches turn-off loss*

The switching turn-off loss can be expressed as

$$P_{turn-off\_loss} = f_s \begin{bmatrix} 2\int_0^{t_c}\left(I_{d\_Q1a} - \dfrac{I_{d\_Q1a}}{t_c}t\right)\left(\dfrac{V_{ds\_Q1a}}{t_c}t\right)dt + \\ 2\int_0^{t_c}\left(I_{d\_Q2} - \dfrac{I_{d\_Q2}}{t_c}t\right)\left(\dfrac{V_{ds\_Q2}}{t_c}t\right)dt + \\ 4\int_0^{t_c}\left(I_{d\_S1} - \dfrac{I_{d\_S1}}{t_c}t\right)\left(\dfrac{V_{ds\_S1}}{t_c}t\right)dt \end{bmatrix} \tag{32}$$

Where I_{d_Q1a} and V_{ds_Q1a} are the current and drain-source voltage of switch Q_{1a} at turned off time, respectively. And t_c is the fall time of the switches.

C. Inductor Loss

1) *Inductor core loss*

The empirical Steinmetz equation is applied to calculate the core loss of the inductor, which is given by

$$P_{L\_core\_loss} = k_L f_s^{\alpha_L} B_{L\_p}^{\beta_L} V_{e\_L} \tag{33}$$

Where k_L = 31.32, α_L = 1.6, and β_L = 1.37 are the Steinmetz coefficients provided by the manufacturer, V_{e_L} is the effective volume of the magnetic core, B_{L_p} is the peak flux density of the inductor, which is expressed as

$$B_{L\_p} = \frac{Li_{L\_max}}{n_L A_{e\_L}} \tag{34}$$

Where n_L is the turns of the inductor, A_{e_L} is the effective area of the magnetic core. Core material and size of inductors are shown as TABLE I.

2) *Inductor copper loss*

The Litz wire is used as the copper material for the two DC inductors and leakage inductor in the converter. The single-turn high-frequency Litz wire is composed of 150 strands of enameled wire, in which the diameter of the single-strand enameled wire is 0.1mm. And the inductor copper loss can be calculated as

$$P_{L\_copper\_loss} = I_{L\_dcrms\_p}^2 R_{L\_dc} + I_{L\_acrms\_p}^2 R_{L\_ac} \tag{35}$$

Where R_{ac_L} is the copper AC resistance of the inductor considering the skin effect, which is expressed as

$$R_{L\_ac} = R_{L\_dc}\Delta\left[\frac{sinh(2\Delta) + sin(2\Delta)}{cosh(2\Delta) - cos(2\Delta)} + \frac{2\left(N_n N_L^2 - 1\right)}{3}\frac{sinh(2\Delta) - sin(2\Delta)}{cosh(2\Delta) + cos(2\Delta)}\right] \tag{36}$$

The first term in (36) describes the skin effect, the second term represents the proximity effect factor [31], [32]. N_n is the number of strands in a bundle for the Litz wire, N_L is the number of bundle layers, Δ is expressed as

$$\Delta = \left(\frac{\pi}{4}\right)^{0.75} \cdot \frac{d_w}{\delta} \cdot \sqrt{0.8} \tag{37}$$

d_w is the diameter of the strand for the Litz wire, δ is the skin depth which is calculated as

TABLE I
Core Material and Size of Inductors.

Inductors	Core Material	Path length L_e (mm)	Cross section A_e (mm^2)	Volume V_e (mm^3)
DC inductors	MPP	81.4 × 2	65.6 × 2	5340 × 2
Leakage inductor	DMR95	57	146	8322

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TABLE II
CORE MATERIAL AND SIZE OF TRANSFORMER.

Core Material	Mn-Zn power ferrite	l_{Width} (mm)	28
l_{Length} (mm)	40	l_{Height}(mm)	40
Effective area (mm^2)	210	Effective volume (mm^3)	19698

TABLE III
CURRENT PARAMETERS COMPARISON.

Item	optimized design		non-optimized case	
Power load	Full load (0.65kW)	Light load (65W)	Full load (0.65kW)	Light load (65W)
DC inductor RMS current i_{Ldc1} or i_{Ldc2} (A)	27.7	6.1	27.7	6.1
Leakage inductor RMS current i_{Lr} (A)	25.23	16.49	31.24	24.57

$$\delta = \sqrt{\frac{2}{2\pi f \mu_0 \sigma_0}} \tag{38}$$

R_{L_dc} is the copper DC resistance of the inductor, which is calculated as

$$R_{L\_dc} = \frac{4 n_L l_L}{N_n \pi d_w^2 \sigma_0} \tag{39}$$

μ_0 is free-air magnetic permeability, l_L is the mean length per turn for the inductor, σ_0 is the electrical conductivity of the copper.

D. Transformer Loss

1) *Transformer core loss*

The standard PQ cores and the Litz wire windings constitute the transformer structure. And the sandwich structure is applied to reduce the leakage inductor of transformer. Core material and size of transformer are shown as TABLE II. The calculation method of the transformer core loss is the same to the inductor core loss, according to the empirical Steinmetz equation. The transformer core loss is calculated as

$$P_{T\_core\_loss} = \frac{k_T f_s^{\alpha_T} B_{T\_p}^{\beta_T} (\mathrm{x} - yT + zT^2) V_{e\_T}}{1000} = P_{V\_T} V_e \tag{40}$$

Where k_T, α_T, and β_T are the Steinmetz coefficients, and the P_{V_T} is power loss density. Both Steinmetz coefficients and power loss density are provided by the manufacturer. However, sometimes the manufacturer only provides the power loss density in the datasheet of transformer for convenience. V_{e_T} is the effective volume of the magnetic core, B_{T_p} is the peak flux density of the transformer, which is expressed as

$$B_{T\_p} = \frac{V_{Cc}(1 - D_{max})}{n_T A_{e\_T} f_s} \tag{41}$$

Where n_T is the primary side turns of the transformer, A_{e_T} is the effective area of the magnetic core.

2) *Transformer copper loss*

The calculation method for the transformer copper loss is the same to the inductor copper loss. The transformer AC resistance is expressed as

$$R_{T\_ac} = R_{T\_dc} \Delta \left[\frac{sinh(2\Delta) + sin(2\Delta)}{cosh(2\Delta) - cos(2\Delta)} + \frac{2(N_n N_L^2 - 1)}{3} \frac{sinh(\Delta) - sin(\Delta)}{cosh(\Delta) + cos(\Delta)} \right] \tag{42}$$

Then the transformer copper loss is expressed as

$$P_{T\_copper} = I_{LVS\_rms}^2 R_{ac\_T\_LVS} + I_{HVS\_rms}^2 R_{ac\_T\_HVS} \tag{43}$$

Where $R_{ac\_T\_LVS}$ and $R_{ac\_T\_HVS}$ are the transformer AC resistance of the primary side winding and secondary side winding, respectively.

E. Current Parameters Comparison

The current parameters comparison between optimized design and non-optimized case under input voltage V_L = 12V are as shown in TABLE III.

F. Power Loss Comparison

To verify the effectiveness of the optimization design, parameters with L_r = 1 μH is used to be the non-optimized case to make the comparison. The loss breakdown comparisions of the converter between the optimized design and non-optimized case at different loads are shown in Fig.10. As Fig.10 (a) shows, when the converter works at light load (120W), the total loss of the non-optimized case is highter than that of the optimized design about 3.89 W. As Fig.10 (b) shows, when the converter works at full load condition (650W), the power loss with the non-optimized case is highter than that of the non-optimized case about 6.94 W. Due to the peak current is high when the switch is turned off and the frequency of switches is high, the turn-off loss is high according to (32). The turn-off loss consists of turn-off of LVS switches and turn-off of HVS switches. And the turn-off currents of the non-optimized case for primary and secondary sides are larger than the optimized design at the switches turn-off time. Thus, the turn-off loss of non-optimized case is large than the optimized design from Fig.10. According to Fig.8(a), RMS currents are different under different values of leakage inductor although ZVS of all switches are achieved independent of leakage inductor. As can be seen, even though ZVS of all switches can be realized, RMS current still decreases with the value of leakage inductance increases near V_L = 12 to 22V. As shown, RMS current with leakage inductance L_r = 1μH is larger than L_r = 1.5μH near V_L = 12 to 22V and peak current of the leakage is also smaller near V_L = 22 to 24V. Switch conduction loss, leakage inductor loss and transformer loss are closely related to RMS current and peak current of leakage inductor. Thus, the total loss of optimized design is smaller than non-optimized case when V_L =12V and V_L =18V. The conclusions coincide with the comparison of efficiency curves

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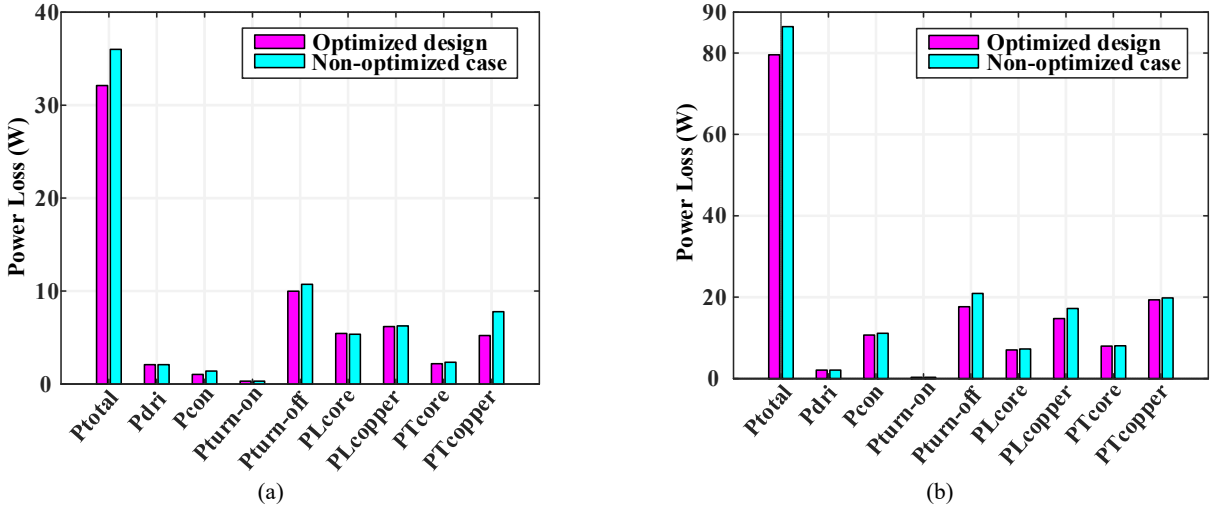

Fig.10. Loss breakdown when V_L = 12 V. (a). at light load (P = 120W). (b). at full load (P = 650W).

TABLE IV
COMPARISON OF RELATED LITERATURES ON BIDIRECTIONAL CONVERTERS

Topology	CF-DAB	Reference [33]	Reference [26]	Reference [34]	Reference [27]	Reference [35]
n_{MOSFETs}	8	6	10	4	8	8
n_{inductor}	3	2	5	2	4	4
$n_{\text{transformer}}$	1	1	1	1	1	1
$n_{\text{capacitor}}$	2	3	5	5	2	2
$G_{step\text{-}up}$ (V_H/V_L)	$n_2/n_1(1\text{-}d)$	$n_1/n_2(1\text{-}d)$^2	$n_1+n_2/n_2(1\text{-}d)$	$n_2/n_1(1\text{-}d)$	$n_2/n_1(1\text{-}d)$	$n_1\sin(D_L\pi)/D_L\sin(D_H\pi)$
Current ripple of V_L	small	medium	small	medium	small	small
ZVS analysis complexity	low	low	high	low	medium	medium
Soft switching range	wide	wide	wide	narrow	wide	wide
Control complexity	low	low	medium	low	high	medium
Parameter design complexity	low	low	medium	low	medium	high

between optimized design and non-optimized case of the converter from Fig.21.

G. Comparison Analysis of Bidirectional Converter

The characteristic comparison of related literatures on bidirectional isolated converters is shown in TABLE IV. n_{MOSFETs} is the number of power switches, n_{inductor} is the number of inductors, $n_{\text{transformer}}$ is the number of transformer, and $n_{\text{capacitor}}$ is the number of capacitors. The converter in [33] has a large input current ripple and high current stress of LVS switches although it has the small voltage surges on switches by the function of leakage inductance energy recovery. The converter in [26] uses voltage multiplier cells to achieve a high conversion ratio, but the analysis of ZVS is complex. The converter in [34] has the disadvantage of large circulation current due to mismatching control of half bridge on primary, secondary sides. In addition, the ZVS range of switch is narrow. ZVS can be achieved for all power switches throughout full range of load even at no-load condition in [27]. However, the working modes are multifarious and control of converter is complex. The converter in [35] can achieved high efficiency. However, the design of resonant tank is difficult.

V. SYSTEM PARAMETERS DESIGN

An experimental prototype has been built in order to verify the effectiveness of the analyses, and it is shown in Fig.11. The system specifications are illustrated in TABLE V. All the design parameters are designed taking into consideration the safe operation of converter for highest loss, i.e., 12V LVS voltage and 650W output power.

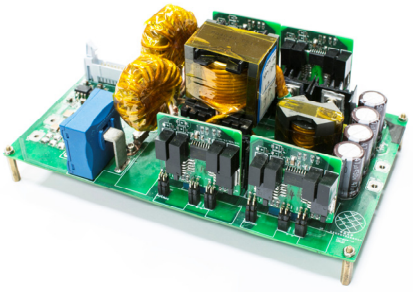

Fig.11. The experimental prototype.

TABLE V.
SYSTEM SPECIFICATIONS

P	650W	L_r	1.5μH
f	100kHz	L_{dc}	5μH
V_L	12~24V	n	5
V_H	240V	C_c	60μF

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A. DC Inductance L_{dc} Design

Firstly, considering the ZVS performance of the LVS switches. According to Fig.6 (a) - (d), the appropriate value range [3μH, 50μH] of L_{dc} can be preliminarily selected. Secondly, the RMS current should be discussed based on the allowed current ripple to obtain the optimized inductance L_{dc} from Fig.9. Taking the ZVS design of the LVS switches, current ripple and RMS current into consideration, L_{eq} is finally designed to be 5μH.

B. Turn Ratio of Transformer Design

The turn ratio of transformer should be designed to ensure the voltage matching control, that is the voltage of clamping capacitor V_{Cc} matches the output voltage V_H. The clamping voltage V_{Cc} = 48V and the output voltage V_H = 240V. According to (5), the turn ratio of transformer is $n = n_2/n_1 = V_H/V_{Cc} = 5$.

C. Leakage Inductance L_r Design

Firstly, the ZVS performance of the HVS switches is affected by the value of the leakage inductance L_r. According to Fig.6 (e) and (f), the appropriate value range [0.5μH, 10μH] of L_r can be preliminarily selected. Secondly, the leakage inductor is closely related to the output power. Thus, $Lr \leq 2.215\mu$H should be satisfied to achieve maximum power transfer form Fig.7. Finally, based on the analysis of RMS current and peak current

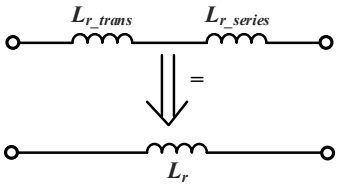

Fig.12. The diagram of leakage inductor.

from Fig.8, the optimized leakage inductor is designed by the tradeoff between RMS current and copper loss. Based on considering the ZVS range, maximum power transfer capability, RMS current and peak current, the leakage inductance L_r = 1.5μH is finally selected.

In the experimental prototype of this paper, the leakage inductor is placed in HVS of converter, that is $L_{rs} = (n_2/n_1)$ ^2 L_r. Through measurement by impedance analyzer, the leakage inductance parameter of primary side and secondary side for the sandwich structural transformer are L_{r_trans} = 0.38μH and L_{rs_trans} = 8.3μH, respectively. Then, the required leakage inductance value is achieved by series connection of an external inductor, that is the leakage inductance L_{rs_trans} of the transformer is compensated by an external series inductance L_{rs_series} to realize the required leakage inductance L_{rs}, as shown in Fig.12.

D. Clamping Capacitor C_c Selection

The selection of the clamping capacitor C_c should ensure that

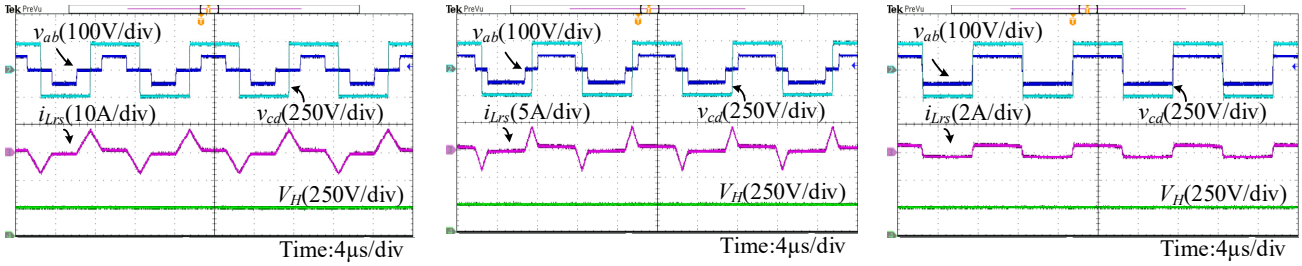

Fig.13. Steady-state waveforms under light load. (a)12V. (b)18V. (c)24V.

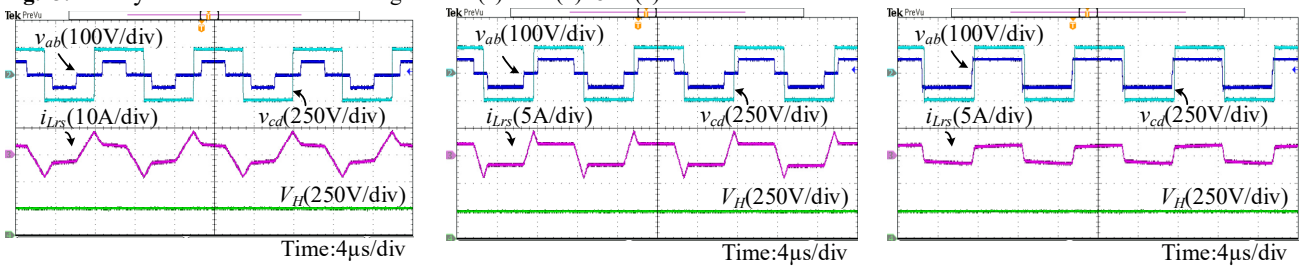

Fig.14. Steady-state waveforms under half load. (a)12V. (b)18V. (c)24V.

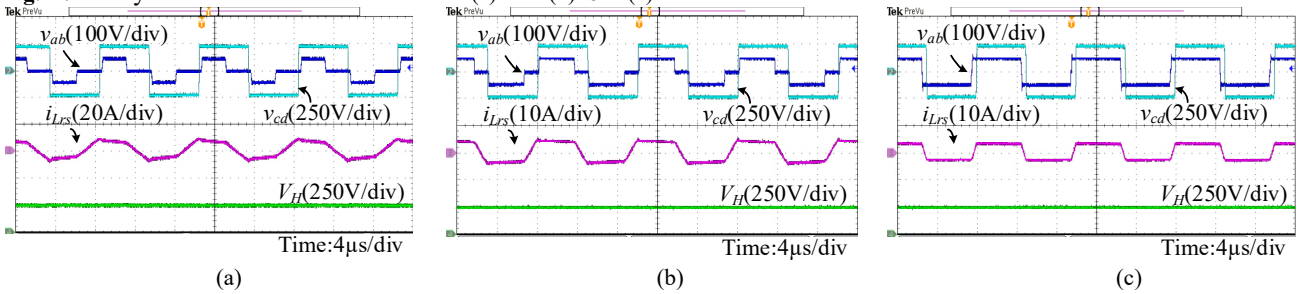

Fig.15. Steady-state waveforms under full load. (a)12V. (b)18V. (c)24V.

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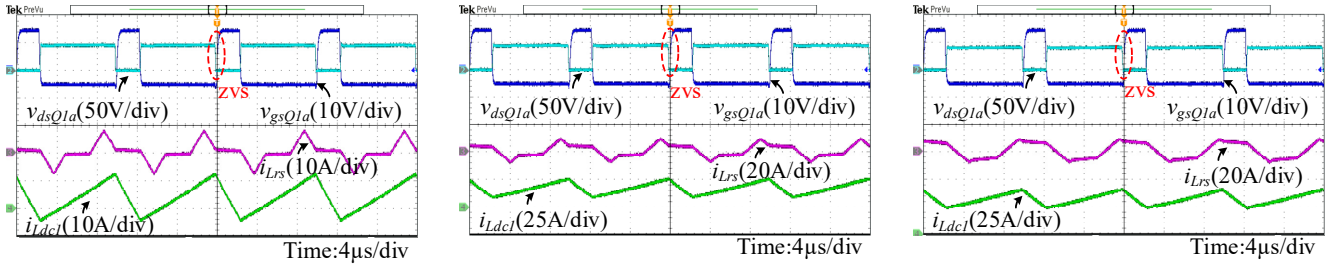

Fig.16. Soft-switching waveforms for Q_{1a}&Q_{2a} when V_L = 12V. (a)light load. (b)half load. (c)full load.

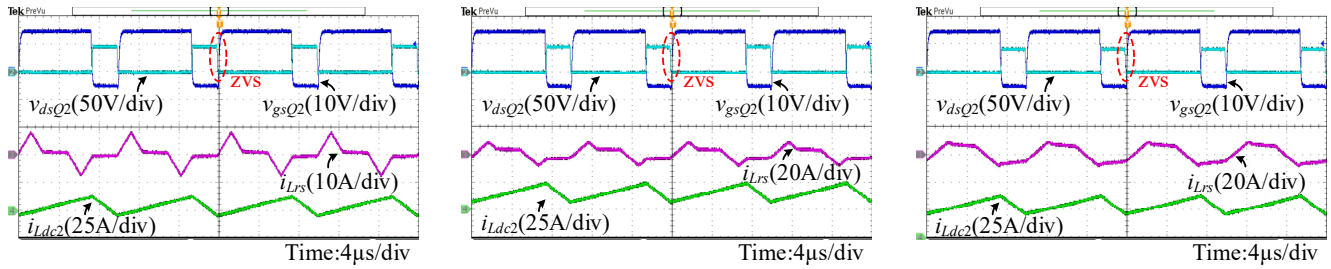

Fig.17. Soft-switching waveforms for Q_1&Q_2 when V_L = 12V. (a)light load. (b)half load. (c)full load.

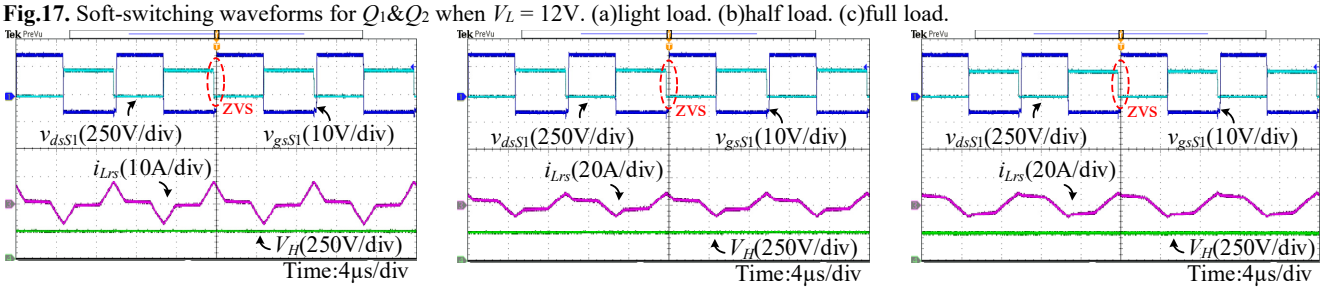

Fig.18. Soft-switching waveforms for S_1&S_2&S_3&S_4 when V_L = 12V. (a)light load. (b)half load. (c)full load.

the voltage ripple across C_c is confined within an allowed range. Due to the complementary of the LVS modulation, only half a switching cycle [t_0, t_6) is analyzed. The clamping voltage $v_{Cc}(t)$ can be calculated by

$$v_{Cc}(t)=\frac{1}{C_c}\int_{t_3}^{t}\left(i_{Ldc1}(t)-i_{Lr}(t)\right)dt+v_{Cc}(t_3) \tag{44}$$

The current $i_{Ldc1}-i_{Lr}$ will charge/discharge Cc. During [t_3, t_4), $i_{Ldc1}-i_{Lr}$ is larger than zero, Cc will be charged and v_{Cc} will rise; while during (t_4, t_6), $i_{Ldc1}-i_{Lr}$ is smaller than zero, Cc is discharged and v_{Cc} will fall. The maximum of v_{Cc} is at t_4, and minimum one is either at t_3 or t_6. So the voltage ripple ΔV_{Cc} across Cc can be illustrated as

$$\Delta V_{Cc}=v_{Cc}(t_4)-\min\left\{v_{Cc}(t_3),v_{Cc}(t_6)\right\} \tag{45}$$

ΔV_{Cc} is designed to satisfy the following criteria:

$$\Delta V_{Cc}/V_{Cc}\le 1\% \tag{46}$$

Calculation for the case of 12V input and 0.65kW load, the critical value for Cc can be obtained

$$C_c\ge 32.7\ \mu\text{F} \tag{47}$$

A near 80% margin is designed. Thus, the clamping capacitor is selected to be 60μF.

E. Switches Selection

The maximum voltage across the LVS switches $V_{Q1\_Q1a\_Q2\_Q2a}$ is the clamping voltage V_{Cc}, that is $V_{Q1\_Q1a\_Q2\_Q2a}$ = 48V. And the maximum voltage across the HVS switches $V_{S1\_S2\_S3\_S4}$ is the output voltage V_H, that is $V_{S1\_S2\_S3\_S4}$ = 240V. The current stresses of LVS switches I_{Q1} = $i_{Ldc1}(t_1)$ - $i_{Lr}(t_1)$ = 63.4A. And the current stresses of HVS switches I_{S1} = $i_{Lr}(t_5)/n_1$= 8A. According to the voltage, current stresses and margin should be considered, device type IPP023N10N5 from Infineon company is selected for the LVS switches, and device type UJ3C065030K3S from United-SiC company is selected for the HVS switches.

VI. Experiment Verification

Fig.13-Fig.15 describe the steady-state waveforms under different loads with different LVS voltages in boost mode. As seen in Fig.13, the converter works at light load under different voltage conditions, in spite of LVS voltage variation, voltage matching can be achieved, that is, the slope of leakage inductor current i_{Lr} is zero in the power transmission stage. The half load and full load steady-state waveforms are shown in Fig.14 and Fig.15 respectively. The phase shift angle exists between v_{ab} and v_{cd}, and it varies with load and LVS voltage V_L. The HVS voltage V_H is fixed in spite of the different loads and V_L.

Fig.16-Fig.18 show the ZVS waveforms of the switches when LVS voltage V_L = 12V under different loads. As can be

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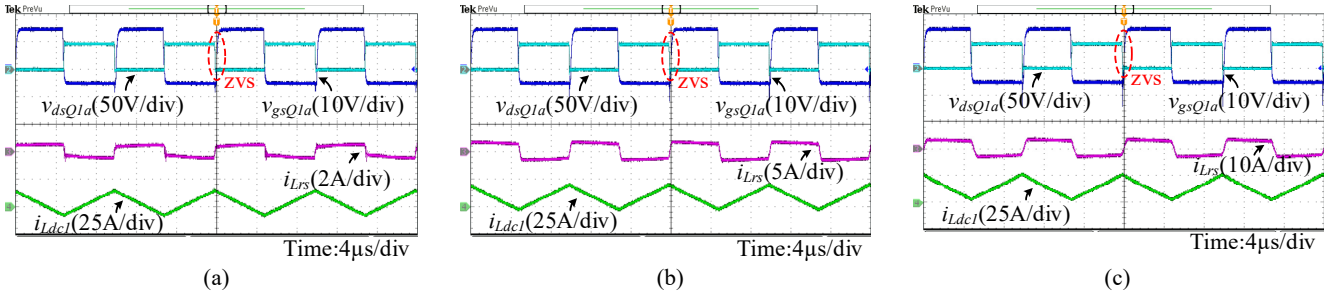

Fig.19. Soft-switching waveforms for Q_{1a}&Q_{2a} when V_L = 24V. (a)light load. (b)half load. (c)full load.

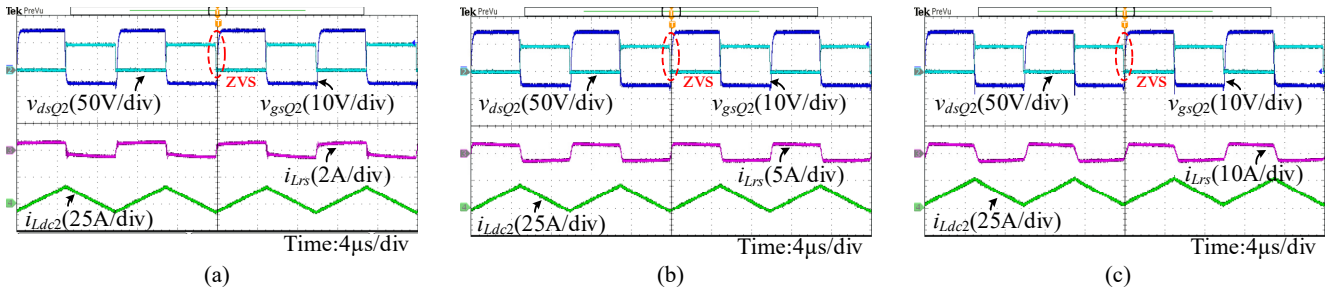

Fig.20. Soft-switching waveforms for Q_1&Q_2 when V_L = 24V. (a)light load. (b)half load. (c)full load.

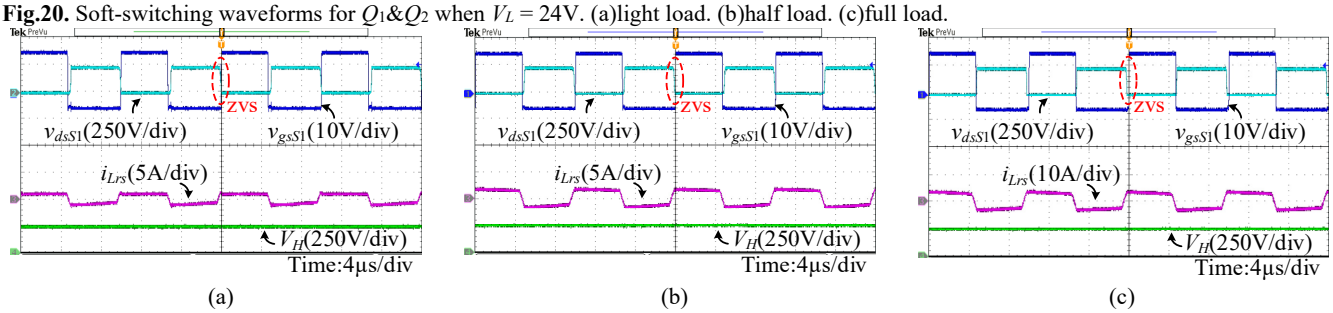

Fig.21. Soft-switching waveforms for S_1&S_2&S_3&S_4 when V_L = 24V. (a)light load. (b)half load. (c)full load.

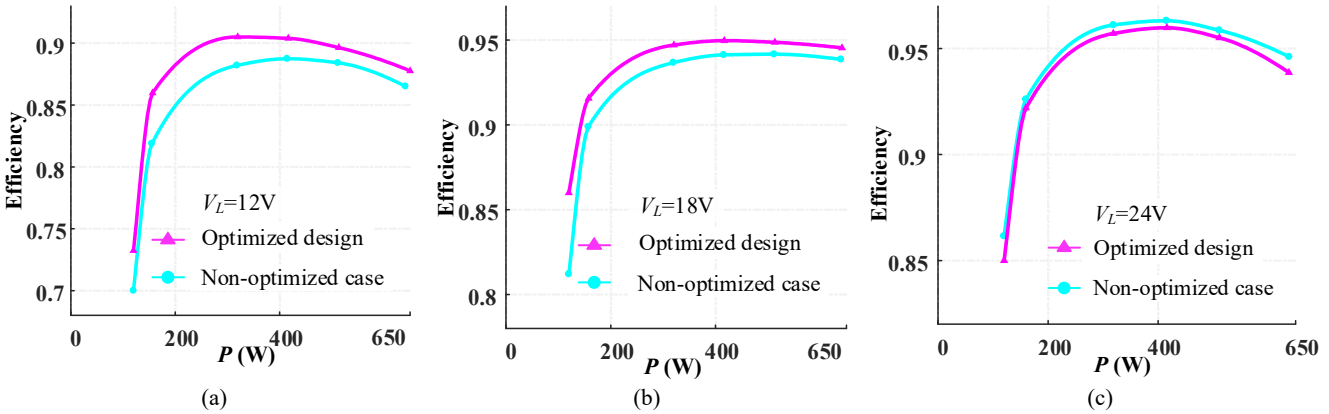

Fig.22. Comparison of efficiency curves between optimized design and non-optimized case of the converter. (a) when V_L=12V. (b) when V_L=18V. (c) when V_L=24V.

seen, ZVS waveforms of the Q_{1a} and Q_{2a} under light load, half load and full load are shown in Fig.16 (a), (b) and (c) respectively, where the drain-source voltage v_{dsQ1a}, date-source voltage v_{gsQ1a} and current i_{Lr}, i_{Ldc1} are given. As seen, ZVS of the LVS upper switches Q_{1a} and Q_{2a} can be achieved at full load range. ZVS waveforms of LVS bottom switches and HVS switches are shown in Fig.17 and Fig.18 respectively. Q_1 and Q_2, S_1-S_4 can achieve ZVS, respectively. Thus all switches can achieve ZVS at full load range when LVS voltage V_L = 12V.

Fig.19-Fig.21 show the ZVS waveforms of the switches when LVS voltage V_L = 24V under different load. As can be seen, all switches can achieve ZVS at full load range when LVS voltage V_L =24V. Thus all switches can achieve ZVS at full load rang with full input voltage range.

The efficiency curves of the prototype using the optimized design and non-optimized case with different LVS voltage and different loads are plotted in Fig.22. The highest efficiency of the optimized design reaches 96% under the 650W load when

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V_L = 24V. As can be seen, at V_L = 12V, when working at light load and full load, the optimized design has better efficiency than the non-optimized case with the different LVS input voltage, which is consistent with the loss breakdown in section IV-F. When V_L =24V, due to the smaller RMS current of leakage inductor, the efficiency of the non-optimized case is slightly higher than the optimized design, but the difference is almost negligible. When the input voltage is 12V or 18V, it can be seen that the efficiency of the optimized design is higher than that of the non-optimized case.

VII. Conclusion and Discussion

In this paper, the working principle of CF-DAB converter under PPS control is analyzed in detail. The voltage matching condition can always be achieved when input voltage varies, which can reduce circulating conduction loss. The ZVS conditions of all switches of the converter are given, and it is proved mathematically that all switches can naturally achieve ZVS independently of DC inductance and leakage inductance under full input voltage range with full load range. In addition, the design of leakage and DC inductances are discussed to achieve relatively low RMS current with the precondition of achieving maximum power transfer. The power loss of the converter of the optimized design is analyzed and total power loss is reduced compared with non-optimized case. The experiment results of the prototype verified the validity of the theoretical analysis. In the future work, the junction capacitor can be added to further analyze the ZVS of all switches.

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