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A single-stage AC-AC solid-state transformer with ZVS operation

Hui Wang[1,2] | **Ming Xu**[1,2] | **Yichun Zhang**[1,2] | **Yao Sun**[1,2] | **Guanguan Zhang**[3] | **Frede Blaabjerg**[4] | **Xiao Liang**[5] | **Yonglu Liu**[1,2] | **Jianghua Feng**[6]

[1] School of Automation, Central South University, Changsha, People's Republic of China

[2] Hunan Provincial Key Laboratory of Power Electronics Equipment and Grid, Changsha 410083, China

[3] School of Control Science and Engineering, Shandong University, Jinan, People's Republic of China

[4] Energy Technology, Aalborg UniversityCentral South University, Aalborg, Denmark

[5] Department of Civil, Structural and Environmental Engineering, University at Buffalo, Buffalo, New York 14260, USA

[6] CSR Research of Electric Technology and Material Engineering, CSR Zhuzhou Electric Locomotive Research Institute Co., Ltd., Zhuzhou, People's Republic of China

Correspondence
Yonglu Liu, School of Automation, Central South University, Changsha, People's Republic of China.
Email: liuyonglu@csu.edu.cn

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Abstract

Solid-state transformer (SST) is an attractive concept, which provides galvanic isolation and voltage scaling by means of a medium-frequency link. In this paper, a single-stage alternative current (AC)-AC SST solution without bulky energy storage elements is presented. The front-end rectifier (FER) and rear-end inverter (REI) of the SST works at line-frequency, while the intermediate LLC series resonant converter (SRC) fulfils the tasks of galvanic isolating and regulating the output voltage. To achieve high efficiency and bidirectional power flow capability of the SST, the zero voltage switching (ZVS) condition of the LLC SRC is comprehensively analysed, and the parameters design method of the LLC SRC is developed, where the resonant currents are constructed by applying the same gating signals to the primary-side and secondary-side bridges and the dead-time is properly selected. Consequently, the presented SST has the merits of high conversion efficiency, naturally bidirectional power flow capability, potentially high power density and high reliability. The experimental results on a 1.5 kW SST prototype show that sinusoidal input and output current, ZVS operation over the full load range are achieved, and the peak efficiency is 97.63%. The experimental results verify the functionality and effectiveness of the developed methods.

1 | INTRODUCTION

Solid-state transformers (SSTs) have the potential to replace the conventional line-frequency transformer (LFT) in many applications, such as in electric traction, renewable energy systems, and smart distribution grids, due to the advantages of multi-functions, faults isolation and flexible connectivity [1–8]. However, issues like low efficiency, low power density, and poor reliability are still major challenges for its industrial applications, and most of the research works aim at addressing these issues.

In fact, the efficiency, power density and reliability features of SSTs depend greatly on the topology structure. Among the numerous presented SST topologies, the alternative current (AC)-direct current (DC)-AC topology is the most commonly used one due to its excellent controllability [9–13]. However, because of the multi-stage conversion structure and the bulky energy storage capacitors, the efficiency, power density and reliability performance of these AC-DC-AC SSTs may degrade. Compared with the AC-DC-AC SSTs, direct AC-AC SSTs are possible to achieve higher efficiency, higher power density and higher reliability due to fewer conversion stages and the absence of energy storage elements [1, 14–22].

In addition to topology structure, soft switching techniques, such as zero voltage switching (ZVS) and zero current switching (ZCS), are also effective measures to improve the efficiency of SSTs. The dual active bridge (DAB) converter has the advantage of good ZVS capability, which is usually adopted as the

DC-DC stage of SSTs. However, the ZVS operation of DAB depends on loads and voltage conditions. Different from DAB, the LLC series resonant converter (SRC) has the merit of load-independent ZVS operation and thus it is considered as an excellent solution for the DC-DC stage of the SSTs. In [22], a current-fed SRC-based SST with wide ZVS ranges is presented. However, bidirectional power flow and output voltage control schemes of the SST, which are of great importance in some applications such as power distribution network, are not involved in this work. In [23] and [24], a modulation scheme to achieve ZVS on both primary and secondary bridges of the SRC is proposed for the AC-DC SST, where a small phase shift between the gating signals of the primary and secondary bridges is introduced, to generate the tiny resonant current required by the ZVS operation of the secondary bridge during the dead-time.

Compared with the AC-DC SST, ZVS operation is more difficult to realize for the direct AC-AC SST, because the voltage across the MOSFETs is time-varying. Besides, there exist high frequency parasitic oscillations during the dead-time caused by the parasitic parameters, such as the output capacitors of the MOSFETs, stray capacitors of the power circuits. The effects of parasitic oscillations cannot be ignored on some occasions because ZVS operation may be affected, especially when the oscillation frequency is close coming to the resonant frequency [24]. In [25], an input-series-output-parallel direct AC-AC SST topology and theoretical analysis for power losses and circuit operation are presented. However, for direct AC-AC SST, considering the time-varying blocking voltage of the MOSFETs and the parasitic oscillations, ZVS condition analysis of a direct AC-AC SST is more complex than that of the AC-DC SST.

A single-stage AC-AC SST solution without bulky energy storage elements is presented here. The circuit operation modes and ZVS conditions of the LLC SRC considering parasitic circuit parameters are analysed in detail. The ZVS condition of the LLC is studied systematically, and the system parameters design method is developed to achieve ZVS and high conversion efficiency over wide load range conditions. A synchronous PWM modulation strategy is presented to realize naturally bidirectional power flow of the LLC without logical switching, and bidirectional power flow capability of the SST is verified experimentally. Besides, the closed-loop control of output voltage is presented to eliminate the effect of grid disturbances such as voltage sag, voltage swell and so on. Therefore, improved output voltage quality of the SST is achieved, which is of great significance for some applications such as power distribution network.

The remainder of this paper is organized as follows: Section II introduces the topology and operating principles of the single-stage AC-AC SST; Section III presents the analysis of operating behaviour and ZVS conditions followed by the design guidelines of the LLC SRC. In Section IV, the control scheme of the SST is developed to achieve a controllable output voltage. Section V shows the experimental results to verify the correctness of the presented methods. Section VI concludes this paper.

2 | THE SINGLE–STAGE AC-AC SST TOPOLOGY AND OPERATING PRINCIPLES

2.1 | The AC-AC SST topology

The circuit diagram of the SST topology is shown in Figure 1 and it consists of a front-end rectifier (FER), a rear-end inverter (REI) and an LLC SRC, where the arrows represent the reference directions of currents. In this topology, both the FER and the REI act as line-commutated converters, whose switching states are only determined by the polarity of the input voltage. The LLC SRC consists of a medium frequency (MF) transformer, primary-side bridge, secondary-side bridge and a resonant tank, which provides galvanic isolation and output voltage regulation. The resonant tank of the LLC SRC is composed of a resonant inductor L_r, a magnetizing inductor L_m and a resonant capacitor C_r. It should be noted that different from the bulky DC-link capacitors in the conventional SSTs, the capacitors C_p and C_s in this topology are small film capacitors used for filtering and commutating. Because there is only one LLC SRC stage that involves high frequency switching, the presented topology in this work is named as "single stage AC-AC SST".

2.2 | Operating principles

For the single-stage SST, the FER and REI are commutated according to the polarity of input voltage. When the input voltage is positive, switches S_1, S_4 of the FER and switches S_{13}, S_{16} of the REI are always on. Otherwise, switches S_2, S_3, S_{14} and S_{15} are turned on. As a result, the sinusoidal input voltage is converted into half-cycle sinusoidal primary-side DC-link voltage, while the half-cycle sinusoidal secondary-side DC-link voltage is transformed into a sinusoidal output voltage.

To achieve ZVS of the primary-side bridge for the LLC SRC, the magnetizing inductance of the MF transformer is designed to generate large enough magnetizing current i_m. Further to ensure ZVS operation of the secondary-side bridge, the gating signals of the secondary-side bridge are the same as that of the primary-side bridge, and the dead-time is specially chosen to construct the required secondary-side resonant current, which is different from the conventional LLC SRC. Figure 2 shows the magnified waveforms of the LLC SRC under forward power flow, where t_d is the dead-time, i_r and i_s are the primary-side and secondary-side resonant currents, t_0 is the starting time of a switching cycle, t_1 and t_2 are the starting time and ending time of the dead-time.

It can be seen from Figure 2 that the phase of i_s leads that of i_r. This is because the magnetizing current i_m is a fixed component irrelevant to the load condition and i_r is decided mainly by i_s. And i_s is determined by the instantaneous output power of the SST. Therefore, when the polarity of the instantaneous output power is positive, i_s leads i_r. Otherwise, i_r leads i_s.

The key waveforms of the single-stage SST are shown in Figure 3, where u_s and i_i are the input voltage and current, u_{dc1}

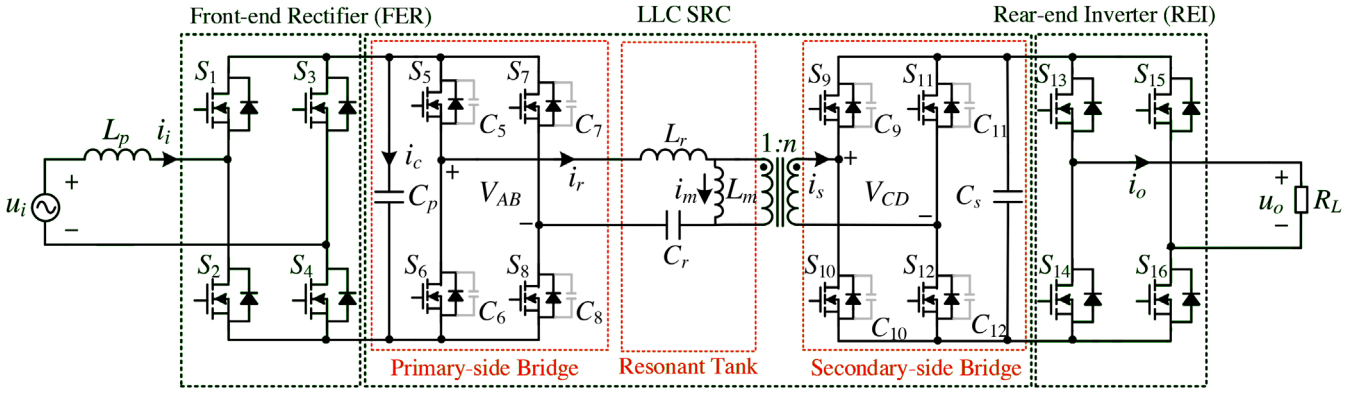

FIGURE 1 The single-stage and single-phase AC-AC solid-state transformer topology

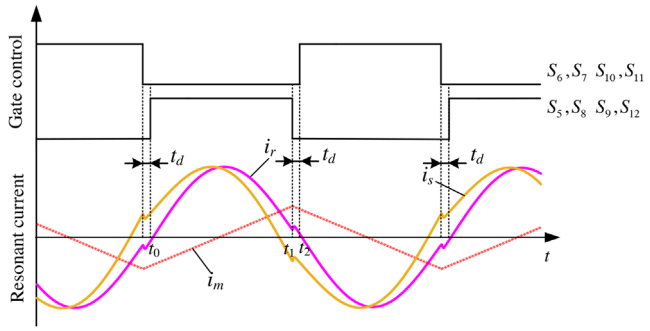

FIGURE 2 Waveforms in the LLC SRC of the SST

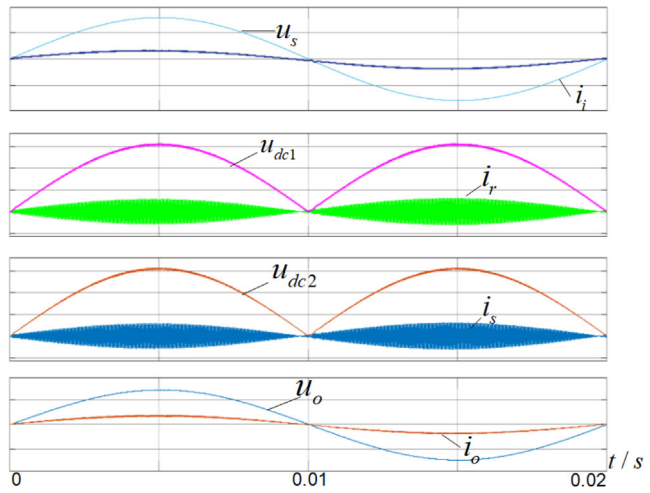

FIGURE 3 The key operating waveforms of the presented SST

and u_{dc2} are the primary-side and secondary-side DC-link voltages, u_o and i_o are the output voltage and current, respectively. As shown in Figure 3, the DC-link voltages are the absolute values of the sinusoidal time-varying waveforms, which means that ZVS operation over the entire input voltage period is a challenge for the presented SST.

3 | OPERATION MODES AND ZVS ANALYSIS OF THE SST

As analysed in Section II and shown in Figure 3, the FER and REI of the SST work at line-frequency, and thus operation modes of the FER and REI are not discussed here. In this section, only the LLC SRC of the SST is analysed in detail. During the dead-time, the resonant currents i_r and i_s oscillate due to the parasitic parameters. Therefore, by designing the system parameters and the dead-time properly, it is possible to utilize the oscillation to achieve ZVS operation by constructing the specific resonant currents in the dead-time.

3.1 | Analysis of the operation modes of the LLC SRC

As shown in Figure 2, there are two modes within a half cycle of the resonant period, and the detailed analysis is given as follows.

Mode 1 [t_0–t_1]: In this mode, the switches S_5, S_8, S_9, S_{12} are on and switches S_6, S_7, S_{10}, S_{11} are off. Before t_0, the primary-side resonant current i_r flows through the body diode of switches S_5 and S_8, while the secondary-side resonant current i_s flows through the body diode of switches S_9 and S_{12}. Then, the output capacitors of switches S_5, S_8, S_9, S_{12} are discharged to zero voltage and switches S_5, S_8, S_9, S_{12} are turned on with zero voltage. During the time interval t_0–t_1, the primary-side resonant current i_r flows through the switches S_5, S_8 while the secondary-side resonant current i_s flows through the switches S_9 and S_{12}. The equivalent circuit in this mode is shown in Figure 4, where the resonant inductor L_r and capacitor C_r participate in the resonance operation. The input and output voltages of the MF transformer V_{AB} and V_{CD} are treated as two voltage sources, and the voltage across the magnetizing inductor is clamped by the secondary voltage V_{CD}.

Mode 2 [t_1–t_2]: In this mode, all switches of the LLC SRC are in the off state. At time $t = t_1$, the switches S_5, S_8, S_9, S_{12} are turned off. The circuit composed by L_r, L_m, C_r and the output capacitors of switches including C_5, C_6, C_7, C_8, C_9, C_{10}, C_{11}, C_{12} start to oscillate. The equivalent circuit in mode 2 is shown

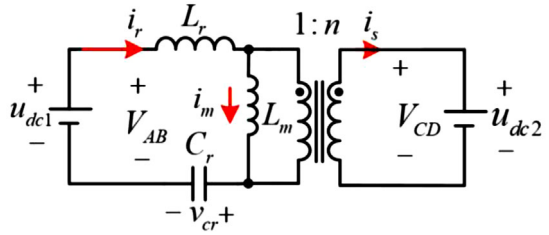

FIGURE 4 Equivalent circuit of mode 1 for the SST

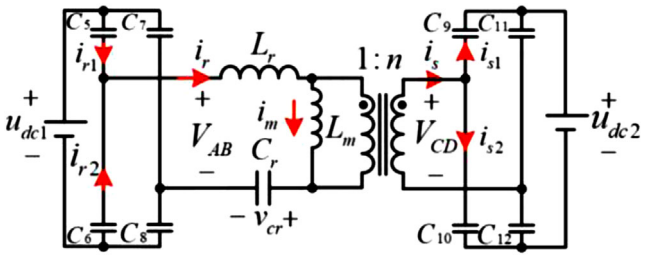

FIGURE 5 Equivalent circuit of mode 2 for the SST

in Figure 5, where i_r is positive and i_s is negative as shown in Figure 2(b). During this interval, i_r discharges C_6, C_7 and charges C_5, C_8, i_s discharges C_{10}, C_{11} and charges C_9, C_{12}, and the voltages across the switches S_6, S_7, S_{10}, S_{11} are zero at time $t = t_2$, consequently, switches S_6, S_7, S_{10}, S_{11} are turned on with zero voltage.

As mentioned previously, the oscillation of i_r is a key factor to achieve ZVS operation, because i_r determines the boundary conditions of ZVS. To obtain the analytical expression of i_r, mathematical models of the LLC SRC with different modes are deduced as follows.

In mode 1, the mathematical model of the resonant tank is written as:

$$L_r \frac{di_r}{dt} = (V_{AB} - V_{CD}/n) - v_{cr} \tag{1}$$

$$L_m \frac{di_m}{dt} = V_{CD}/n \tag{2}$$

$$C_r \frac{dv_{cr}}{dt} = i_r \tag{3}$$

where v_{cr} is the voltage across the resonant capacitor C_r. According to Equations (1)–(3), i_r is derived as:

$$i_r(t) = i_r(t_0)\cos\omega_r(t - t_0) + \frac{\Delta V - v_{cr}(t_0)}{Z_r}\sin\omega_r(t - t_0) \tag{4}$$

where $i_r(t_0)$ is the value of i_r at time $t = t_0$, $v_{cr}(t_0)$ is the value of v_{cr} at time $t = t_0$, $\Delta V = V_{AB} - \frac{V_{CD}}{n}$, $\omega_r = \frac{1}{\sqrt{L_r C_r}}$ and $Z_r = \sqrt{\frac{L_r}{C_r}}$.

In mode 2, the output capacitors of the switches, C_r, L_r and L_m participate in the resonance process, where the mathematical model of the LLC SRC is expressed as:

$$\begin{cases} i_r = i_{r1} + i_{r2} \\ i_s = i_{s1} + i_{s2} \\ i_r = i_m + n i_s \\ V_{AB} = u_{c7} - u_{c5} \\ V_{CD} = u_{c11} - u_{c9} \end{cases} \tag{5}$$

$$\begin{cases} C_5 \frac{du_{C5}}{dt} = -C_7 \frac{du_{C7}}{dt} = i_{r1} \\ C_6 \frac{du_{C6}}{dt} = -C_8 \frac{du_{C8}}{dt} = -i_{r2} \\ C_{11} \frac{du_{C11}}{dt} = -C_9 \frac{du_{C9}}{dt} = i_{s1} \\ C_{10} \frac{du_{C10}}{dt} = -C_{12} \frac{du_{C12}}{dt} = i_{s2} \end{cases} \tag{6}$$

where u_{C5}, u_{C6}, u_{C7}, u_{C8}, u_{C9}, u_{C10}, u_{C11}, u_{C12} are the voltages across the capacitors C_5, C_6, C_7, C_8, C_9, C_{10}, C_{11}, C_{12}, respectively.

Equations (1, 2) and (3) are also valid for mode 2. The output capacitor of the switch is non-linear, and the capacitance of the output capacitor increases with the decrease of the voltage across the switch. Therefore, for the single-stage SST, it is difficult to realize ZVS near the zero cross point of the input voltage. Despite all this, the switching losses of the switch near the zero cross point of input voltage can be ignored because both the voltage across switch and the resonant current are very small. To simplify the theoretical analysis, we assume that the capacitance of the output capacitor of the switches is identical and the capacitance is C_{oss}, $i_{r1} = i_{r2}$ and $i_{s1} = i_{s2}$. Then Equation (1) can be deduced as:

$$L_r \frac{d^2 i_r}{dt^2} + \frac{dv_{cr}}{dt} = \frac{d(V_{AB} - V_{CD}/n)}{dt} \tag{7}$$

According to Equations (5) and (6), the resonant capacitor voltage is written as:

$$\begin{aligned} \frac{d\Delta V}{dt} &= \frac{d((u_{C7} - u_{C5}) - (u_{C11} - u_{C9})/n)}{dt} \\ &= -i_r \frac{1}{C_{oss}} - i_s \frac{1}{nC_{oss}} \end{aligned} \tag{8}$$

Substituting Equations (3) and (8) into Equation (7), the relationship between the currents i_r and i_s is given as:

$$L_r \frac{d^2 i_r}{dt^2} + \frac{i_r}{C_r} = -i_r \frac{1}{C_{oss}} - i_s \frac{1}{nC_{oss}} \tag{9}$$

Combining Equations (2) and (5), the second-order differential model of the MF transformer is:

$$L_m \frac{d^2(i_r - n i_s)}{dt^2} = i_s \frac{1}{nC_{oss}} \tag{10}$$

Then, the fourth-order differential model of i_r is calculated by Equations (9) and (10) as,

$$L_m L_r n^2 C_{oss} \frac{d^4 i_r}{dt^4} + \left(L_m n^2 (C_{oss}/C_r + 1) + L_m + L_r\right) \frac{d^2 i_r}{dt^2} + (1/C_r + 1/C_{oss}) i_r = 0 \quad (11)$$

According to Equation (11), the general solution of i_r can be derived as

$$i_r(t) = \lambda_1 \sin \omega'_{rs}(t - t_1) + \lambda_2 \cos \omega'_{rs}(t - t_1) + \lambda_3 \sin \omega_{rs}(t - t_1) + \lambda_4 \cos \omega_{rs}(t - t_1) \quad (12)$$

and ω_{rs} and ω_{rs}' are expressed as:

$$\omega_{rs} = \sqrt{\frac{\beta + \sqrt{\beta^2 - 4\alpha\gamma}}{2\alpha}}, \omega'_{rs} = \sqrt{\frac{-\beta + \sqrt{\beta^2 - 4\alpha\gamma}}{2\alpha}} \quad (13)$$

where $\alpha = L_m L_r n^2 C_{oss}$, $\beta = L_m n^2 (C_{oss}/C_r + 1) + L_m + L_r$, and $\gamma = 1/C_r + 1/C_{oss}$.

According to Equations (1), (5) and (9), the first to third order differential models of i_r are deduced as:

$$\begin{cases} i_r'(t_1) = \frac{1}{L_r}(V_{AB}(t_1) - \frac{V_{CD}(t_1)}{n} - V_{cr}(t_1)) \\ i_r''(t_1) = i_m(t_1) \frac{1}{n^2 C_{oss} L_r} - i_r(t_1) \frac{1}{L_r}(\frac{1}{n^2 C_{oss}} + \frac{1}{C_{oss}} + \frac{1}{C_r}) \\ i_r'''(t_1) = i_m'(t_1) \frac{1}{n^2 C_{oss} L_r} - i_r'(t_1) \frac{1}{L_r}(\frac{1}{n^2 C_{oss}} + \frac{1}{C_{oss}} + \frac{1}{C_r}) \end{cases} \quad (14)$$

Combining Equations (15) and (12), the specific solution of i_r is solved as:

$$i_r(t) = \lambda_1 \sin \omega'_{rs}(t - t_1) + \lambda_2 \cos \omega'_{rs}(t - t_1) + \lambda_3 \sin \omega_{rs}(t - t_1) + \lambda_4 \cos \omega_{rs}(t - t_1) \quad (15)$$

$$\begin{cases} \lambda_1 = -\frac{i_r'''(t_1) + \omega_{rs}^2 i_r'(t_1)}{\omega'_{rs}\left(\omega'^2_{rs} - \omega_{rs}^2\right)} \\ \lambda_2 = -\frac{i_r''(t_1) + \omega_{rs}^2 i_r(t_1)}{\omega'^2_{rs} - \omega_{rs}^2} \\ \lambda_3 = \frac{i_r'''(t_1) + \omega'^2_{rs} i_r'(t_1)}{\omega_{rs}\left(\omega'^2_{rs} - \omega_{rs}^2\right)} \\ \lambda_4 = \frac{i_r''(t_1) + \omega'^2_{rs} i_r(t_1)}{\omega'^2_{rs} - \omega_{rs}^2} \end{cases} \quad (16)$$

3.2 | Analysis of the ZVS conditions

To fulfil ZVS condition of the primary-side bridge, the primary-side resonant current direction should remain unchanged during the dead-time, to ensure full discharge of the output capacitors of the switches before turn-on. Similarly, to achieve ZVS operation of the secondary-side bridge, the direction of the secondary-side current should also remain unchanged during the dead-time. Therefore, half of the resonant current oscillation period should be longer than the dead-time, which is $t_d < \pi/\omega_{rs}$. From Equation (13), the upper limit of the dead-time is calculated as:

$$t_d < \pi \sqrt{\frac{2\alpha}{\beta + \sqrt{\beta^2 - 4\alpha\gamma}}} \quad (17)$$

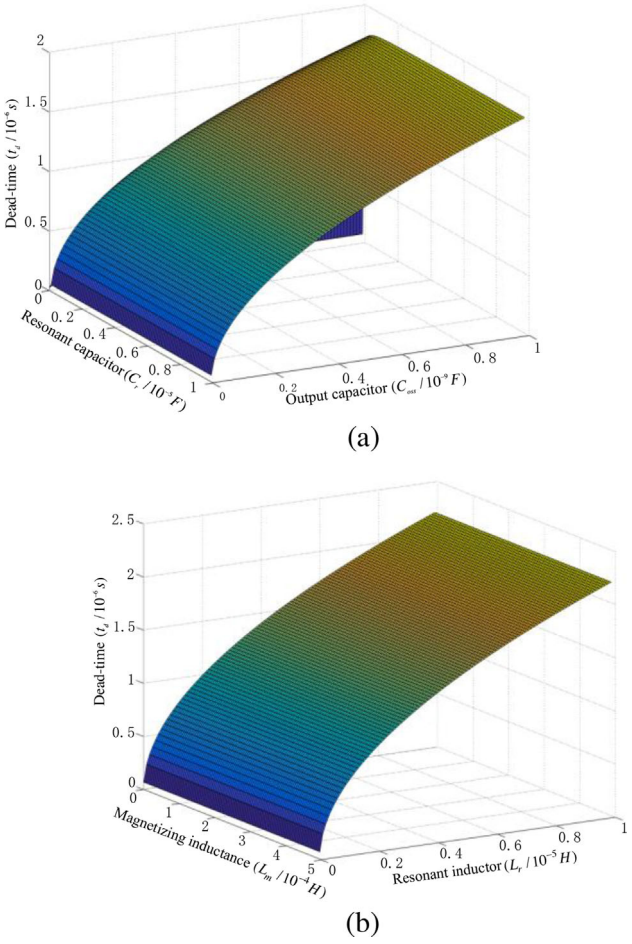

FIGURE 6 The upper limit of the dead-time versus system parameters (a) C_r and C_{oss}, for $L_r = 6.8$ μH, $L_m = 90$ μH; (b) L_r and L_m, for $C_r = 0.9$ μF, $C_{oss} = 1$ nF

The upper limit of the dead-time versus different system parameters is plotted in Figure 6. As shown in Figure 6, the oscillation frequency is not sensitive to the resonant capacitor C_r and the magnetizing inductor L_m while it is sensitive to the resonant inductor L_r and the output capacitor C_{oss}. The oscillation frequency increases with the decrease of L_r and C_{oss}.

To realize the ZVS operation of the primary-side bridge, the output capacitor of the switches should be fully discharged, and its condition is expressed as:

$$\int_{t_1}^{t_2} i_r(t)dt > 2Q_{ossp} + C_{strayp} U_{im} |\sin(\omega_i t)| \quad (18)$$

where C_{strayp} is the lumped stray capacitor across the primary-side resonant tank, U_{im} is the amplitude of the input voltage, Q_{ossp} is the charge of the output capacitor of the primary-side switch and it is expressed as:

$$Q_{ossp} = k_a\sqrt{U_{im}|\sin(\omega_i t)|} + k_b U_{im}|\sin(\omega_i t)| \tag{19}$$

where k_a and k_b are the specific parameters associated with the switches. Equation (18) can be further deduced as:

$$\begin{aligned}&\frac{\lambda_2\sin\omega'_{rs}t_d-\lambda_1\cos\omega'_{rs}t_d}{\omega'_{rs}} + \frac{\lambda_4\sin\omega_{rs}t_d-\lambda_3\cos\omega_{rs}t_d}{\omega_{rs}}\\ &>2Q_{ossp}+C_{strayp}U_{im}|\sin(\omega_i t)|\end{aligned} \tag{20}$$

It should be noted that the capacitance of the output capacitor depends on the voltage across the switch. However, Equation (17) is still valid for non-linear capacitance. In fact, to achieve ZVS we only need to ensure that the direction of the resonant current does not change and the output capacitors are fully discharged during the dead-time.

Similarly, for the secondary-side bridge, the ZVS condition is given as:

$$\int_{t_1}^{t_2} -i_s(t)dt > 4Q_{osse}+C_{strayse}U_{om}|\sin(\omega_i t)| \tag{21}$$

where Q_{osse} is the charge of the output capacitor of the secondary-side switch and $C_{strayse}$ is the lumped stray capacitor across the secondary-side circuit; U_{om} is the amplitude of the output voltage of the SST.

Because the dead-time is small, the magnetizing current i_m is considered constant during the dead-time. Then, the secondary-side ZVS condition is given as:

$$\int_{t_1}^{t_2} \frac{i_m(t_1)-i_r(t)}{n}dt > 4Q_{osse}+C_{strayse}U_{om}|\sin(\omega_i t)| \tag{22}$$

And the secondary-side ZVS condition can be derived further as:

$$\begin{aligned}&\frac{1}{n}(i_m(t_1)t_d - \frac{\lambda_2\sin\omega'_{rs}t_d-\lambda_1\cos\omega'_{rs}t_d}{\omega'_{rs}}\\ &-\frac{\lambda_4\sin\omega_{rs}t_d-\lambda_3\cos\omega_{rs}t_d}{\omega_{rs}})\\ &>2Q_{ossp}+C_{strayp}U_{im}|\sin(\omega_i t)|\end{aligned} \tag{23}$$

In this case, once the SST system parameters are given, ZVS is achieved when Equations (17), (20) and (23) are satisfied.

3.3 | System parameters designing

In all, the design guideline of the LLC SRC is given as follows. The first step is to determine the switching frequency, because the switching frequency is vital to the performance of the LLC SRC. Although a low frequency helps to decrease the switching losses of the converter, it results in a large volume of the transformer and capacitors. A high frequency is beneficial to improve the power density of LLC SRC, but it leads to large losses of the power conductors and the transformer's magnetic core and increases the system EMI concerns. Then, according to the switching frequency and the rated resonant current, the resonant inductor and resonant capacitor could be selected. The resonant inductor affects the amplitude of the resonant current and the resonant capacitor is constraint by the voltage across it. As shown in Figure 6, the upper limit of the dead-time is sensitive to the resonant inductor, thus it should also be taken into consideration. Finally, to achieve ZVS operation, the magnetizing inductor and dead-time are designed according to Equations (17), (20) and (23). As shown in Equations (20) and (23), the ZVS constraint is determined by the resonant current and the dead-time, while the dead-time is constraint by the magnetizing inductor. When the magnetizing inductor is close to the resonant inductor, it will affect the upper limit of the dead-time dramatically.

The design guidelines for the DC link capacitors C_p and C_s are discussed as follows.

For the discussed topology in this work, the upper limit of the capacitance of the DC-link capacitor C_p and C_s is mainly determined by the expected input power factor:

$$(C_p + n^2C_s) < \frac{P_{in}}{\omega_{in}V^2_{in(RMS)}}\tan\phi \tag{24}$$

where ϕ, P_{in}, ω_{in} and $V_{in(RMS)}$ are the rated input power factor angle, the rated input active power, angular frequency of the input voltage and the rated input RMS voltage, respectively.

On the other hand, the lower limit of the capacitance of the DC-link capacitors is determined by the allowable voltage ripples across C_p and C_s. As can be seen from Figure 1, during the positive half cycle of the input voltage, the current of C_p can be written as:

$$i_c = i_i - i_r \tag{25}$$

$$i_i = I_{im}\sin(\omega_{in}t) \tag{26}$$

where I_{im} is the amplitude of input current. The voltage ripple of C_p can be solved by integrating the capacitor current

$$\Delta u_c = \frac{1}{C_p}\int_{t_0}^{t_1} i_c dt \tag{27}$$

And the voltage ripple can be deduced further as:

$$\Delta u_c = \frac{1}{C_p}\left(I_{im}\frac{2\sin(\omega_{in}/2f_s)\sin(\omega_{in}(t_0+t_1))}{\omega_{in}} + \frac{I_r}{\omega_r}\right) \tag{28}$$

Define the voltage ripple coefficient as

$$\lambda_p=\frac{\Delta u_c}{u_{dc1}}=\frac{1}{C_p V_{in}}\left(\frac{2I_{im}\sin(\omega_{in}/2f_s)}{\omega_{in}}+\frac{I_{im}}{2f_s}\right) \tag{29}$$

where ω_{in} is the input voltage frequency, f_s is the switching frequency of LLC resonant converter. Then, the lower capacitance limit of C_p is expressed as:

$$C_p>\frac{\frac{2I_{im}\sin(\omega_{in}/2f_s)}{\omega_{in}}+\frac{I_{im}}{2f_s}}{\lambda_p V_{in}} \tag{30}$$

For the secondary-side DC link capacitor C_s, the lower limit of the capacitance can be solved in a similar way.

In this work, with the constraints of the rated input power factor ≥ 0.99 and the capacitor voltage ripple coefficient $\leq 10\%$, the primary-side DC link capacitor C_p and the secondary-side DC link capacitor C_s are both selected as 3.3 μF.

As can be seen from the above design guideline for the DC link capacitors, the capacitance of the DC link capacitors is close to that of the resonant capacitor. Therefore, the influence of the DC link capacitors on the resonant frequency should be examined carefully. Based on the time domain analysis tool, the analysis of the influence of the DC link capacitors on the resonant process is given as follow.

To solve the resonant current i_r, the time domain equation can be derived as:

$$\frac{d^2 i_r}{dt^2}+\frac{1}{L_r}\left(\frac{1}{C_p}+\frac{1}{C_s}+\frac{1}{C_r}\right)i_r=\frac{1}{L_r}\left(\frac{1}{C_p}+\frac{1}{C_s}\right)i_i \tag{31}$$

The analytical solution of resonant current can be derived as:

$$i_r(t)=\begin{cases} I_r\sin\left(\frac{t}{\sqrt{L_r C_{rs}}}-\varphi\right)+\left(\frac{C_{rs}}{C_{res}}\right)i_i, 0\leq t\leq T_{re}/2 \\ I_r\sin\left(\frac{t}{\sqrt{L_r C_{rs}}}-3\varphi\right)-\left(\frac{C_{rs}}{C_{res}}\right)i_i, T_{re}/2\leq t\leq T_{re}\end{cases} \tag{32}$$

where $C_{rs}=\frac{1}{\frac{1}{C_p}+\frac{1}{C_s}+\frac{1}{C_r}}$, $C_{res}=\frac{1}{\frac{1}{C_p}+\frac{1}{C_r}}$; I_r, $\varphi$and T_{rep} represent the magnitude, initial phase and actual resonant period of the resonant current i_r.

To solve the initial phase φ, the equation of resonant current zero-cross point is written as:

$$i_r(0)=-I_r\sin(\varphi)+\left(\frac{C_{rs}}{C_{res}}\right)i_i=0 \tag{33}$$

According to the Equation (33), the current i_i can be expressed as:

$$i_i=I_r\sin(\varphi)\times\frac{C_{res}}{C_{rs}} \tag{34}$$

Besides, the resonant capacitor voltage amplitude can be derived by power balance

$$\Delta V_{cr}=\frac{P}{4u_{dc1}f_{re}C_r} \tag{35}$$

where f_{re} is the actual resonant frequency.

The resonant capacitor voltage amplitude can also be solved by integrating the resonant current

$$\Delta V_{cr}=\frac{1}{C_r}\int_0^{T_{re}/4} I_r\sin\left(\frac{t}{\sqrt{L_r C_{rs}}}-\varphi\right)+\left(\frac{C_{rs}}{C_{res}}\right)i_i dt \tag{36}$$

Combine Equations (35) and (36), the following equation can be obtained:

$$-\frac{I_r}{C_r}\sqrt{L_r C_{rs}}\left(\cos\left(\frac{T_{re}/4}{\sqrt{L_r C_{rs}}}-\varphi\right)-\cos(-\varphi)\right)+\frac{1}{C_r}\left(\frac{C_{rs}}{C_{res}}\right)i_i\times\frac{1}{4f_{re}}=\frac{u_i i_i}{4u_{dc1}f_{re}C_r} \tag{37}$$

According to Equations (33) and (37), the initial phase φcan be derived as:

$$\frac{2}{\pi+2\varphi}\cos(\varphi)=\sin(\varphi)\times\frac{C_{res}}{C_{rs}}\left(1-\frac{C_{rs}}{C_{res}}\right) \tag{38}$$

For the designed system parameters in this work, the initial phase is solved as$\varphi=0.227$. Therefore, the actual resonant frequency f_{re} can be calculated as:

$$f_{re}=\frac{\pi}{(\pi+2\varphi)}\frac{1}{2\pi\sqrt{L_r C_{rs}}}=66.5\text{kHz} \tag{39}$$

which is a bit higher than the ideal resonant frequency f_r defined by:

$$f_r=\frac{1}{2\pi\sqrt{L_r C_r}}=64.3\text{kHz} \tag{40}$$

4 | OUTPUT VOLTAGE REGULATION OF THE SST

For the SST, since the REI works at line-frequency, the LLC SRC undertakes the task of AC output voltage regulation. For the forward mode, the voltage transfer function of the LLC SRC, described as the relationship between the primary-side DC-link voltage u_{dc1} and the secondary-side DC-link voltage u_{dc2} [26–29], is written as:

$$G_{gain}=\left|\frac{L_n f_n^2}{\left[(L_n+1)f_n^2-1\right]+j\left[\left(f_n^2-1\right)f_n Q_s L_n\right]}\right| \tag{41}$$

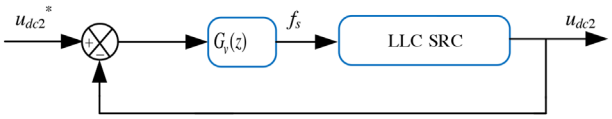

FIGURE 7 Output voltage control scheme for the SST

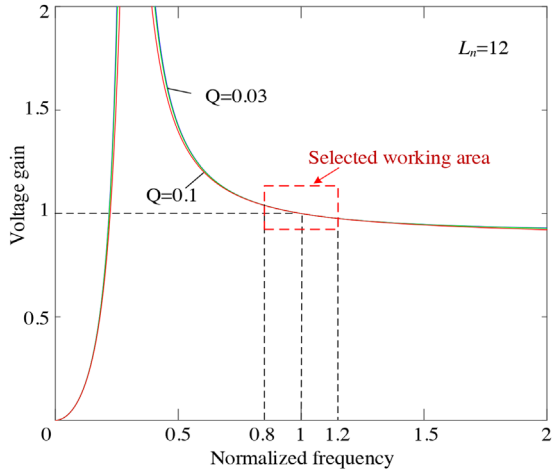

FIGURE 8 Voltage gain versus the normalized frequency

where f_n is the normalized frequency and $f_n = f_s/f_r$, f_s is the switching frequency; $L_n = L_m/L_r$ is the normalized inductance, Q_s is the quality factor of the LLC SRC and $Q_s = \sqrt{L_r/C_r}/R_L$, R_L is the equivalent load resistor of the LLC SRC.

According to Equation (41), the voltage transfer gain is determined by Q_s, L_n and f_n, and the output voltage of LLC can be regulated by changing the switching frequency.

Then, the voltage control scheme based on the conventional frequency-domain method is developed as shown in Figure 7, where u_{dc2}^* is in phase with u_{dc1} and its amplitude is the same as the desired AC output voltage, LLC SRC tracks the reference voltage u_{dc2}^* by adjusting the switching frequency. For the target of a 500 Hz bandwidth and a 0.707 damping ratio for the control system, the discrete voltage feedback compensation is designed as:

$$G_v(z) = -\frac{6.834\times10^{-9} + 4.653\times10^{-9}z^{-1} - 2.751\times10^{-10}z^{-2}}{1 - 1.965z^{-1} + 0.9653z^{-2}}$$

with a control frequency of 20 kHz.

When the system parameters are settled, the range of frequency control is restricted by the resonant frequency, and L_n is determined by the magnetizing inductance. According to Equation (24), to meet the requirements of ZVS operation, the normalized inductance L_n is selected as 12, and the voltage gain versus the normalized frequency is shown in Figure 8. To meet the regulation demand and maintain the switching frequency within the proper range, the normalized frequency is designed as 0.8–1.2.

TABLE 1 System parameters of the SST

System parameters	Value
Output rated power P_o	1.5 kW
Input rated voltage u_i	220 V_{rms}
Input frequency ω_i	314 rad/s
Rated output voltage u_o	220 V_{rms}
LLC resonant frequency f_r	66.5 kHz
Dead time t_d	0.8 μs
Input inductor L_p	200 μH
Capacitor C_p	3.3 μF
Resonant inductor L_r	6.8 μH
Resonant capacitor C_r	0.9 μF
Turns ratio n	1
Magnetizing inductance L_m	90 μH
Capacitor C_s	3.3 μF
Load resistor R_o	32 Ω

As has been presented in [28], the LLC converter becomes a LC SRC when it runs in reverse power flow direction, and the mode and voltage transfer function are different from that of the forward case. Though the output voltage control framework in Figure 7 is valid for both the forward and reverse power flow directions, the switching frequency range as well as the controller parameters in reverse power flow should be redesigned [27]. For simplicity the detailed analysis and design for the reverse power flow case are not elaborated here.

In essence, the magnitude of the fundamental component of the resonant converter that determines the secondary-side DC link voltage, is the only control objective from the perspective of the first harmonic approximation (FHA) theory. Since the secondary-side DC link voltage pulsates at twice the line frequency (100 Hz), a 20 kHz control frequency is sufficient to achieve good control performance of the secondary-side DC link voltage as well as the output voltage of the SST.

5 | EXPERIMENTAL RESULTS

To validate the correctness of the presented methods, a 1.5 kW prototype with the system parameters shown in Table I is built, as shown in Figure 9. The switches of the FER and REI are 600 V/72 mΩ MOSFETs (FCH072N60F) due to its low conduction losses, and the control platform is DSP TMS320F28069.

5.1 | Experiments

Figure 10 shows the input and output waveforms of the SST under full load condition, where the load of the SST is a 32 Ω resistor. The upper waveforms are the input voltage u_i and the input current i_i, while the bottom waveforms are the output

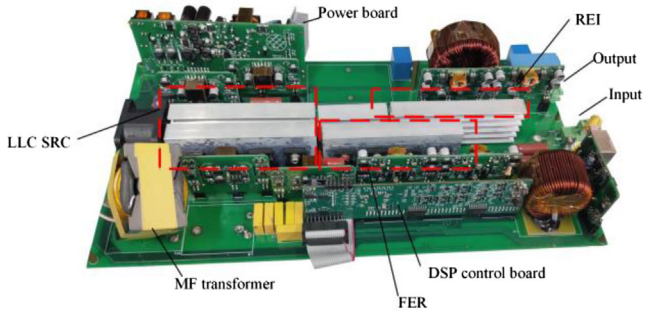

FIGURE 9 Prototype of the presented SST

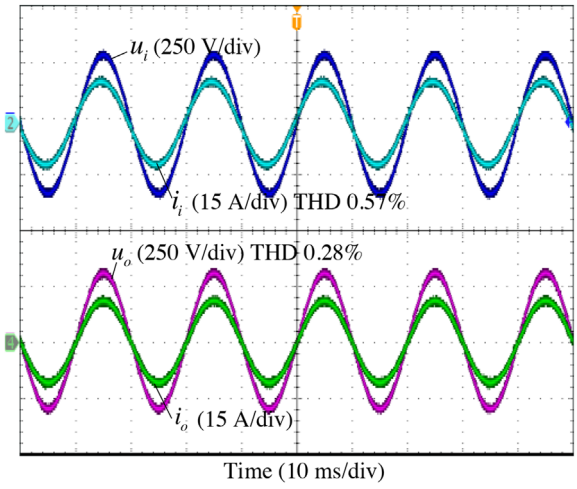

FIGURE 10 Steady-state waveforms of the input and output of the SST under forward power flow direction

voltage u_o and the output current i_o. It shows that the input current is sinusoidal and in phase with the input voltage, also both the output voltage and the output current are sinusoidal. The total harmonic distortion of the input current and output voltage are 0.57% and 0.28%, respectively.

To demonstrate the bidirectional power flow capability of the SST, an external grid connected single phase inverter is selected as the load of the SST in the next tests, and the output power, as well as the power flow direction of the SST are changed by setting the active and reactive components of the grid-connected current of the external grid-connected inverter. And in the whole tests the output of the SST is controlled as a voltage source.

Figure 11 shows the waveforms of the SST with the external grid-connected inverter load, where the input power factor of the external grid-connected inverter is non-unity and the power flow direction of the SST is forward. As shown in Figure 11, the output voltage still tracks the desired AC output voltage well, and the input current of the SST is sinusoidal but is not in phase with the input voltage. This is because of the uncontrollability of the FER, the input current of the SST is indirectly synthesized by the output current and thus the phase angle of the input current is the same as that of the output current.

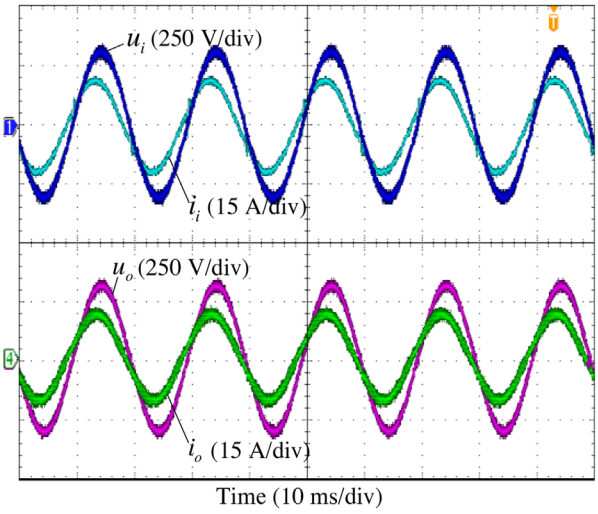

FIGURE 11 Steady-state waveforms of the input and output of the SST under the non-unity input power factor

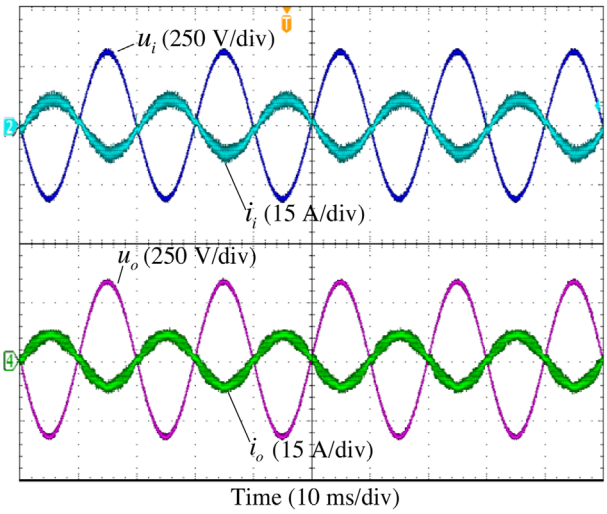

FIGURE 12 Steady-state waveforms of the input and output of the SST under reverse power flow direction

Figure 12 shows the waveforms of the SST under reverse power flow direction, where a pure minus active component of the desired grid-connected current is set for the external grid-connected inverter. As shown in Figure 12, the output voltage and input current are still sinusoidal, and the input current is out of the phase with the input voltage, demonstrating the reverse power flow of the SST. Therefore, sinusoidal input current and output voltage, and bidirectional power flow capability are achieved in the SST. Besides, it can be seen that the input and output current quality of the SST in Figure 12 is poorer than that in Figure 10. This is because when the external grid connected inverter is used as the load, the output current of the SST (also the input current of the external grid connected inverter) contains high frequency harmonic components generated by the external grid connected inverter. Therefore, the input and output current quality of the SST when feeding the

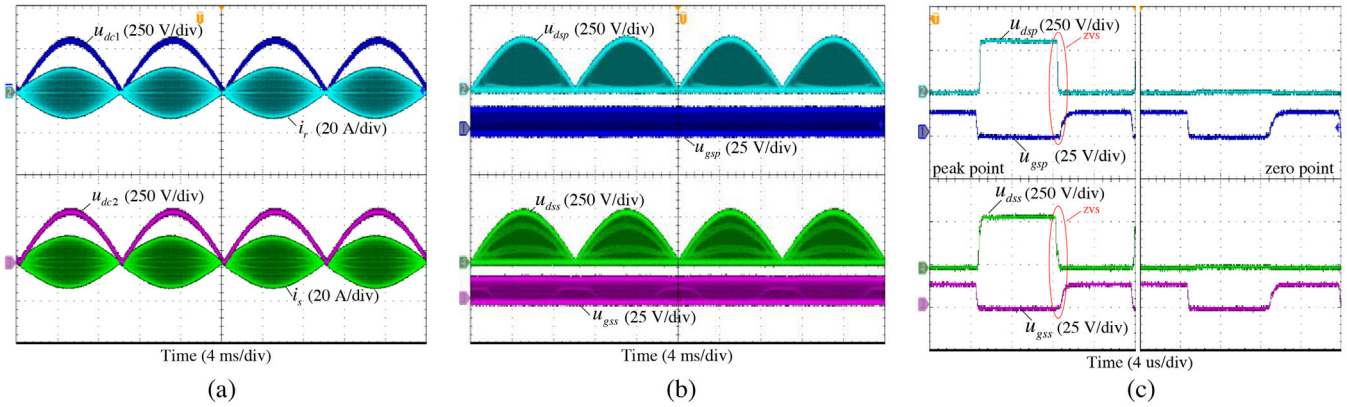

FIGURE 13 Experimental waveforms of the LLC SRC under 1 kW load condition: (a) DC-link voltage and resonant currents of the primary-side and secondary-side. (b) Drain to source voltages and gate to source voltages of primary-side and secondary-side bridges. (c) Magnified view of the drain to source voltages and gate to source voltages of primary-side and secondary-side bridges at the peak point and zero point of the input voltage

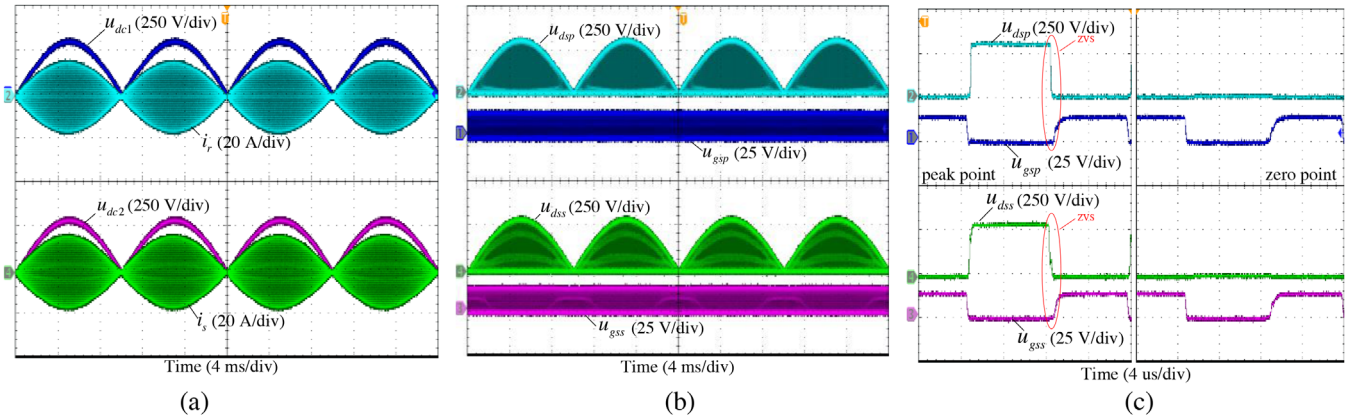

FIGURE 14 Experimental waveforms of the LLC SRC under 1.5 kW load condition. (a) DC-link voltage and resonant currents of the primary-side and secondary-side. (b) Drain to source voltages and gate to source voltages of primary-side and secondary-side bridges. (c) Magnified view of the drain to source voltages and gate to source voltages of primary-side and secondary-side bridges at the peak point and zero point of the input voltage

external grid connected inverter is inferior to that of the resistor load inevitably.

Figures. 13 and 14 show the waveforms of the LLC SRC under 1 and 1.5 kW load, respectively, where u_{dsp} and u_{gsp} are the drain to source voltage and gate to source voltage of the primary-side; u_{dss} and u_{gss} are the drain to source voltage and gate to source voltage of the secondary-side. As shown in Figure 13(a,c), the DC-link voltage is shaped as the absolute value of the sinusoid waveform, and the envelope of the resonant current is in phase with the input voltage. From Figure 13(c) and Figure 14(c), both the falling edge of the drain-to-source voltage of the primary-side and the secondary-side MOSFETs precede the rising edge of gate-to-source voltage of the MOSFETs. For the presented SST, because the primary-side DC-link voltage varies from 0 to 311 V in a line cycle, these results demonstrate that ZVS operation of LLC SRC is achieved in wide input voltage and load ranges.

Figure 15 shows the output voltage regulation capability of the SST. Figure 15(a) shows the input and output waveforms when the input voltage drops to 0.9 times of the rated value. For the conditions of the input voltage rising to 1.1 times of the rated value, Figure 15(b) shows the results of input and output waveforms. As can be seen from Figure 15, the output voltage achieves the rated value of 220 V_{rms} with the developed output voltage control method, which demonstrates the effectiveness of the output voltage control method.

5.2 | Efficiency evaluation

In this part, first, the power losses and system efficiency are calculated. Then the practical efficiency of the prototype is measured by a HIOKI 3390 power analyser and is compared with the calculated one and the matrix-type SST discussed in [21].

Since the FER and REI are commutated at line frequency, the power losses are mainly the conduction losses. The total power losses of the FER and REI, denoted as P_{lossp}, is expressed as:

$$P_{\mathrm{lossp}} = (2I_{\mathrm{i}}^2 + 2I_{\mathrm{o}}^2)R_{\mathrm{on}} + P_{\mathrm{lossL}} \tag{42}$$

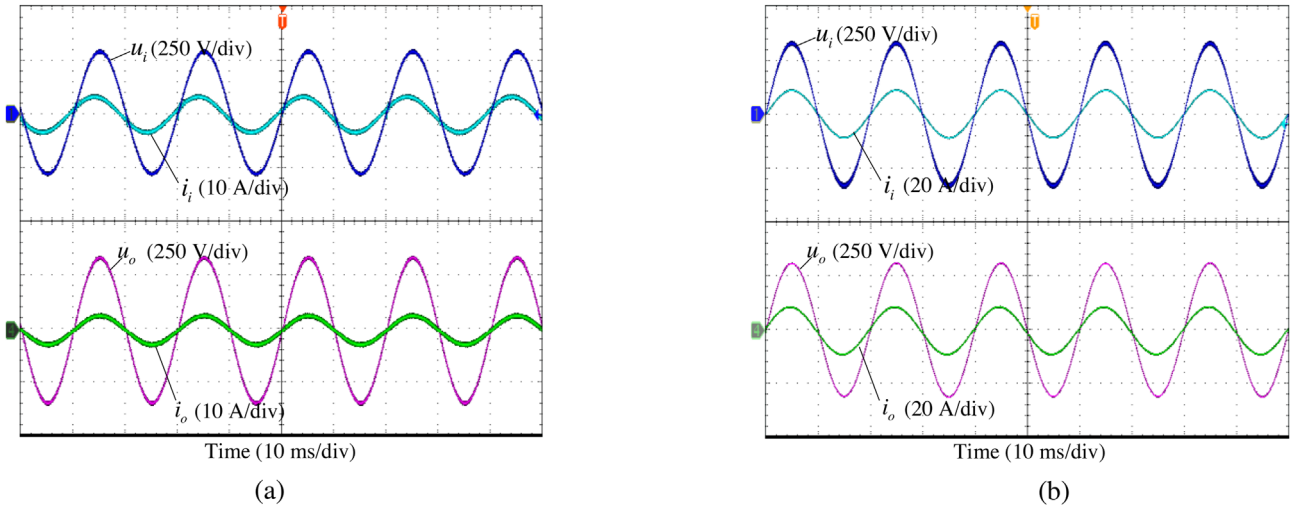

FIGURE 15 Input and output waveforms. (a) u_i is 0.9 times of the rated voltage. (b) u_i is 1.1 times of the rated voltage

where P_{lossL} is the losses of input filter inductor calculated as $P_{lossL} = I_i^2 R_{cui} + P_{coreloss}$, R_{cui} is the resistance of the input filter inductor and $P_{coreloss}$ is the core loss of input filter inductor; I_i and I_o are the input and output RMS currents, respectively; R_{on} is the on-state resistance of the switches of the FER and REI.

For the LLC SRC, since ZVS is achieved for both sides and the turn-off currents of the LLC SRC are small, the power losses of the LLC SRC are mainly the conduction losses which are calculated as:

$$P_{lossLLC} = \frac{2}{\pi}\int_0^{\pi} (I_r^2 R_{on-p} + I_s^2 R_{on-s}) d\theta + P_{losst} \quad (43)$$

where $R_{on\text{-}p}$ and $R_{on\text{-}s}$ are the on-state resistance of the primary-side and secondary-side bridge switches, respectively; I_r and I_s are the primary-side and secondary-side resonant RMS currents, respectively; P_{losst} is the total loss of MF and the resonant capacitor. Thus, the efficiency of the presented SST prototype is,

$$\eta = 1 - \frac{P_{lossp} + P_{lossLLC} + P_{aux}}{P_{in}} \quad (44)$$

where P_{aux} is the power provided by the auxiliary power supply.

Figure 16 shows the comparative results of the calculated and measured efficiencies and the efficiency of the matrix-type SST in [21].

As shown in Figure 16, because of the lower switching losses of the inversion stage, the efficiency of the presented AC-AC SST is obviously higher than that of the work presented in [21]. Furthermore, it can be seen that the measured efficiencies are in good agreement with the calculated ones, and the measured peak efficiency is 97.63%; the efficiency of the actual prototype under rated load condition is measured as 96.21%. It is satisfactory for a small power rating AC-AC SST.

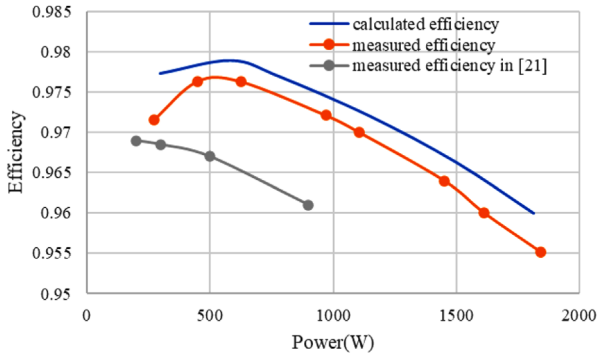

FIGURE 16 Efficiency evaluation of the presented SST

6 | CONCLUSION

In this paper, the ZVS conditions and design guidelines of the single-stage AC-AC SST solution without bulky energy storage elements are analysed comprehensively. By applying the same gating signals to the switches of the primary and secondary sides and designing the system parameters properly, natural bidirectional power flow capability and ZVS operation over wide input voltage and load ranges are achieved. The presented closed-loop control of the output voltage can eliminate the effect of grid disturbances. As a result, high output voltage quality of the SST is achieved. The experimental results verify the effectiveness of the presented methods, and the peak efficiency reaches 97.63%. Due to its advantages such as high conversion efficiency, natural bidirectional power flow capability, controllable output voltage, high power density, and improved output voltage quality, the AC-AC SST is an attractive candidate for many applications such as power distribution network.

ORCID

Frede Blaabjerg https://orcid.org/0000-0001-8311-7412
Xiao Liang https://orcid.org/0000-0003-4788-8759
Yonglu Liu https://orcid.org/0000-0003-4046-446X

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