A New Modulation Strategy to Reduce Common Mode Current of Indirect Matrix Converter

Mei Su, Jianheng Lin, Yao Sun, and Shiming Xie

Abstract—This letter presents a new space vector modulation (SVM) strategy adopting new zero vectors to achieve common mode current (CMC) reduction for indirect matrix converter (IMC). By substituting conventional zero vectors by new zero vectors, the impedance of common mode loop increases, which contributes to CMC reduction. Thus, the IMC system with proposed method alleviates the adverse effects of CMC for AC drives. Moreover, additional hardware and complex commutation process are not required. Experiments are conducted to verify the effectiveness of the proposed method.

Index Terms—Common-mode current (CMC), indirect matrix converter (IMC), space vector modulation (SVM), zero vector.

I. INTRODUCTION

MATRIX converter (MC) is a direct AC/AC converter, and it could be divided into direct matrix converter (DMC) and indirect matrix converter (IMC). Since MC has the advantages of bidirectional power flow, controllable input power factor, arbitrary amplitude and frequency of load voltage, and no DC-link component [1-3], it has been widely employed for motor drive, power supply, wind power generation and other areas [4-6].

As other pulse width modulation (PWM) inverters, the switching actions of MC in motor drive systems will generate common mode voltage (CMV), which has been the main influence factor on the operation of high-power PWM drive [7]. Besides, the common mode current (CMC) due to CMV in the drive system may generate electromagnetic interferences (EMIs), which will disturb the surrounding electronic equipment [8]. Therefore, it is important to reduce the adverse effects of CMC within the power converter. Researchers have focused on two main solutions to mitigate the harmfulness of CMC. The first solution is using additional hardware such as a passive filter or active filter in order to reduce common mode conducted emissions [9-10]. However, this solution would need additional hardware components and make the entire system bulkier and expensive. The second one is to develop new pulse width modulation (PWM) strategies for IMC [11-14]. Due to the advantages of low cost and ease of implementation, the second solution is more promising.

The early space vector pulse width modulation (SVPWM) for MC and IMC were proposed in [15] and [16]. All of them did not focus on CMC issue. As CMV reduction is beneficial for CMC mitigation, many modulation schemes are presented to reduce CMV. Conventional zero vectors always lead to large CMV, thus zero vectors have become focus of attention for CMV reduction. In [11], two active vectors with opposite directions are used to replace zero vectors and another two active vectors are used to produce reference output voltage. This method is effective over the entire range of modulation index but it results in additional switching loss and output current quality is affected. In [12], zero vectors in the inverter stage of IMC are eliminated and three adjacent active vectors are used to synthesize the desired output voltage vector. However, its working area is constrained with high voltage transfer ratio greater than 0.577. In [13], only six rotating input voltage vectors are applied to DMC without zero vectors. This method can obtain zero CMV, but its voltage transfer ratio is limited from 0 to 0.5 and harmonic content of output currents increases. In [14], a modulation method where no zero vectors but two active vectors operate in the inverter stage is proposed. Similarly, it is also limited by voltage transfer ratio. Moreover, its commutation process is complex. In summary, the drawbacks of voltage transfer ratio limitation or higher switching loss exist in the abovementioned SVM strategies for CMV reduction.

Recently, model predictive control (MPC) strategy has been introduced to reduce CMV. In [17], a predictive control scheme for IMC is proposed for CMV attenuation, where CMV has been incorporated into the cost functions. In [18], a model predictive control method is proposed for DMC to achieve zero CMV, in which only six rotating vectors are candidates for control inputs. Compared with SVM-based CMV reduction method, MPC is greatly dependent on parameter accuracy and computation speed. Also, SVM has the advantage of greater

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flexibility to reduce switching loss and CMV. Therefore, SVM is a better choice for CMV reduction in IMC.

To reduce CMC, this letter proposes a new space vector modulation strategy. The essence of this modulation strategy is adopting new zero vectors to replace the conventional zero vectors. In contrast, the new zero vectors would increase the impedance of common mode loop. Therefore, the CMC in IMC can be reduced significantly. Besides, the adoption of new zero vectors does not complicate the commutation process. Moreover, this method is also applicable to other power converters which have similar structure with IMC. The correctness and effectiveness of the proposed modulation strategy are verified by experimental results.

II. PROPOSED SVM METHOD TO REDUCE CMC FOR IMC AND THE PERFORMANCE ANALYSIS

The IMC topology shown in Fig. 1 consists of rectifier stage and inverter stage. The rectifier stage is a bidirectional current source rectifier (CSR) which takes charge of producing a virtual DC-link voltage as well as sinusoidal input currents. And the inverter stage is a voltage source inverter (VSI) which generates desired output voltages.

![Fig. 1. Topology of the indirect matrix converter.](image)

**A. Proposed SVM Method**

The space vector diagrams for the SVM are shown in Fig. 2, where six active vectors ($\mathbf{a}$, $\mathbf{b}$, or $\mathbf{c}$) divide the complex plane into six sectors, respectively. Without loss of generality, consider the desired input current vector lying in sector I ($\varphi_i \in [0, \pi/3]$), as shown in Fig. 2(a). This reference input current space vector is generated by using two adjacent active vectors and one zero vector, the duty ratios of active vectors are given by

$$
\begin{align*}
  d_{m1} &= m_i \sin(\varphi_i - \varphi_i) \\
  d_{m2} &= m_i \sin(\varphi_i)
\end{align*}
$$

where $\varphi_i$ is corresponding angle between the first vector and reference vector, and $m_i$ denotes the rectifier modulation index which ranges from 0 to 1.

![Fig. 2. Space vector diagrams for SVM algorithm. (a) Space vectors of CSR. (b) Space vectors of VSI.](image)

As shown in Fig. 2(b), assume that the desired output voltage vector is also located in sector I ($\theta_s \in [0, \pi/3]$), the corresponding duty ratios of the used vectors are

$$
\begin{align*}
  d_{s1} &= m_s \sin(\varphi_s - \theta_s) \\
  d_{s2} &= m_s \sin(\theta_s)
\end{align*}
$$

where $\varphi_s$ is corresponding angle between the first vector and reference vector, and $m_s$ denotes the inverter modulation index which ranges from 0 to 1.

This proposed method assigns the zero vectors originally applied to the inverter stage to the rectifier stage. And the most important thing is that new zero vectors are used to replace the conventional zero vectors which are never been used in conventional methods. The new defined zero vectors are generated by turning off all the rectifier-stage switches and letting the inverter stage switches being in any active vector. Since the inverter stage has six active vectors, there are six new zero vectors in all and they are listed in Table I. Fig. 3 illustrates the switching state of $V_{z1}$.

![Fig. 3. Switch action diagram of new zero vector $V_{z1}$.](image)

**TABLE I NEW DEFINED ZERO VECTORS**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>($S_1S_2S_3S_4S_5S_6$)</th>
<th>($S_{ap}S_{bp}S_{cp}S_{ap}S_{bp}S_{cp}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{z1}$</td>
<td>(0,0,0,0,0,0)</td>
<td>(1,0,0,0,1,1)</td>
</tr>
<tr>
<td>$V_{z2}$</td>
<td>(0,0,0,0,0,0)</td>
<td>(1,1,0,0,0,1)</td>
</tr>
<tr>
<td>$V_{z3}$</td>
<td>(0,0,0,0,0,0)</td>
<td>(0,1,0,1,0,1)</td>
</tr>
<tr>
<td>$V_{z4}$</td>
<td>(0,0,0,0,0,0)</td>
<td>(0,1,1,1,0,0)</td>
</tr>
<tr>
<td>$V_{z5}$</td>
<td>(0,0,0,0,0,0)</td>
<td>(0,0,1,1,1,0)</td>
</tr>
<tr>
<td>$V_{z6}$</td>
<td>(0,0,0,0,0,0)</td>
<td>(1,0,1,0,1,0)</td>
</tr>
</tbody>
</table>

The average dc-link voltage would be lower than conventional methods. However, the proposed method still remains the maximum range of voltage transfer ratio which...
ranges from 0 to 0.866 because the new zero vectors do not affect output capacity of IMC compared with conventional zero vectors.

Combine the rectifier and inverter modulation process, the proposed switching pulse in one switching period is shown in Fig. 4 and $d_0$ can be expressed as

$$d_0 = 1 - d_1 d_2 - d_1 d_3 - d_2 d_3 - d_1 d_3 d_2.$$  \hspace{1cm} (3)

As can be seen from Fig. 4, during each switching cycle, all three-phase bridge arms of the rectifier stage need to be switched but only one bridge arm of the inverter stage need to be switched. Compared with conventional SVM method, the number of switching states in the inverter stage is reduced significantly. However, the switching commutation times of the rectifier stage increase. Thus, this method changes distribution of system switching loss. Because the zero vectors are eliminated from the inverter stage, the peak value of CMV can be reduced which is beneficial for CMC mitigation [19].

It is worth noting that the arrangement of the new zero vectors must follow a certain rule. The rule in this paper is as follows. When the desired output voltage vector is located in sector I, the zero vector is $V_{z1}$; while in sector II, the used zero vector is $V_{z2}$. In the other sectors, the zero vector is chosen in a similar fashion.

Assume the desired output voltage vector is located in sector I, the switching sequence is shown in Fig. 4. It can be found that inverter stage is always under voltage vector $V_{0}$ (100) when all the rectifier stage switches are turned off. That is to say, only zero vector $V_{z1}$ is used in this case. According to Fig. 3, it can be found that the zero vector is valid if and only if a-phase load current is greater than zero (load current $I_{ma}$ flows into motor). Otherwise, $I_{ma}$ will flow into the clamp circuit [16] of IMC, which is an undesired state. According to Fig. 5, the valid working area lies on the right half plane of Fig. 5(b) when the desired output voltage vector is located in sector I. According to the analysis before, it can be concluded that the proposed modulation is feasible when the angle between output voltage vector and output current vector is in $[-30^\circ, 90^\circ]$. Thus, the modulation scheme is suitable for the loads such as induction motor or PMSM. During large transients such as startup or shutdown, the angle between output voltage and output current may exceed the feasible working area for a short time. To deal with this issue, the conventional modulation method could be used to replace the proposed one temporarily. After the large transients disappear, the proposed modulation scheme would work again. As the harm to motor due to the common mode current is a long-term result, the temporary mode switching will not influence the effect of the proposed modulation method.

### B. Analysis of Equivalent Common Mode Circuit

Fig. 6 shows the equivalent common mode circuit of the IMC system in Fig. 1, where $L_I$ is the inductance of input filter, $C_p$ is the equivalent common mode parasitic capacitance of the switches in the rectifier stage (all the switches are off), $L_{in}$ and $R_m$ are the common-mode impedance of three-phase stator winding, $C_m$ is the equivalent stray capacitances between the motor windings and motor frame [9]. And $u_{com}$ is the common mode voltage which can be expressed as

$$u_{com} = \frac{u_{in} + u_{ho} + u_{cm}}{3}.$$  \hspace{1cm} (4)

When the matrix converter works under any active vector, switch S in Fig. 6 is in position 1; while the converter works under any new zero vector, switch S is in position 2. However, if the conventional modulation methods are applied, the switch S will always be in position 1. According to circuit theory, in position 1, the CMC is the sum of zero-input response and zero-state response. While in position 2, the CMC is only zero-input response, and the common mode impedance is greater than that in position 1. Therefore, CMC could be reduced compared to conventional methods.

### III. EXPERIMENTAL RESULTS

To verify effectiveness of the proposed control strategy experimentally, a prototype of IMC is built in the laboratory as shown in Fig. 7. The specifications of this system are summarized in Table II. High speed insulated gate bipolar transistor (IGBT) IHW30N120R2 (1200V/30A, Infineon) is used in the prototype. All the bidirectional switches in the rectifier stage are made up of two IGBTs with common emitter. Since the IMC has lots of switches and the DSP has limited PWM output ports, the combination of a floating-point DSP (TMS320F28335) and a field programmable gate array (FPGA EP2C8J144C8N) is adopted which are integrated in the controller board. An induction motor is selected as control target.

![Laboratory prototype of the IMC system.](image)

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The rectifier modulation index $m_t$ is set to 1 and the inverter modulation index $m_r$ is set to 0.7. Output frequency is selected as 40Hz. The coaxial PMSM connected with resistors (50Ω) is used to simulate the loads. Fig. 8(a) and (b) show the experimental waveforms of dc-link voltage $u_{com}$, common mode current $i_{com}$ and load current $i_m$ with conventional SVM method and proposed SVM method. As observed, the waveforms of the dc-link voltage are different.

Its main reason is that the conventional method utilizes two large line voltages to synthesize the dc-link voltage, whereas the proposed method also applies one zero vector to the rectifier stage modulation process so that the dc-link voltage is synthesized by three line voltages and one of them is nearly zero. Also, it is obvious that the peak-to-peak values of CMV and CMC in Fig. 8(b) are smaller than those in Fig. 8(a).

As shown in Fig. 9, there exists a small phase difference between the line current and phase voltage, whose main reason is that the reactive current of input filtering capacitors still accounts for a large proportion. Besides, the line current and output line voltage of these two methods are the same basically, and the little distortion of input current is caused by inappropriate design of input filter. To compare the current quality of these two methods, the comparisons of THD at the input and output sides are summarized in Table IV. According to Table IV, the adoption of new zero vectors would not affect input and output performance.

### TABLE II

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$u_{in}$</td>
<td>Input line voltage</td>
<td>220 V(rms)</td>
</tr>
<tr>
<td>$\omega_0$</td>
<td>Input angular frequency</td>
<td>314 rad/s</td>
</tr>
<tr>
<td>$L_p$</td>
<td>Input filter inductance</td>
<td>0.6 mH</td>
</tr>
<tr>
<td>$C_f$</td>
<td>Input filter capacitance</td>
<td>30 μF</td>
</tr>
<tr>
<td>$R_f$</td>
<td>Damping resistance</td>
<td>6 Ω</td>
</tr>
<tr>
<td>$N_p$</td>
<td>Number of pole pairs</td>
<td>2</td>
</tr>
<tr>
<td>$R_s$</td>
<td>Stator resistance</td>
<td>6.4 Ω</td>
</tr>
<tr>
<td>$R_r$</td>
<td>Rotor resistance</td>
<td>4.8 Ω</td>
</tr>
<tr>
<td>$L_m$</td>
<td>Mutual inductance</td>
<td>0.5 mH</td>
</tr>
<tr>
<td>$L_s$</td>
<td>Stator inductance</td>
<td>0.575 mH</td>
</tr>
<tr>
<td>$L_r$</td>
<td>Rotor inductance</td>
<td>0.575 mH</td>
</tr>
<tr>
<td>$T_s$</td>
<td>Modulation period</td>
<td>100 μs</td>
</tr>
</tbody>
</table>

### TABLE III

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td>CMV RMS</td>
<td>59.72 V</td>
<td>65.84 V</td>
<td>65.30 V</td>
<td>77.46 V</td>
</tr>
<tr>
<td>Peak-Peak</td>
<td>370 V</td>
<td>368 V</td>
<td>360 V</td>
<td>392 V</td>
</tr>
<tr>
<td>CMC RMS</td>
<td>9.80 mA</td>
<td>11.95 mA</td>
<td>10.32 mA</td>
<td>11.87 mA</td>
</tr>
<tr>
<td>Peak-Peak</td>
<td>86 mA</td>
<td>100 mA</td>
<td>102 mA</td>
<td>104 mA</td>
</tr>
</tbody>
</table>

### TABLE IV

<table>
<thead>
<tr>
<th>Method</th>
<th>Input current</th>
<th>Output current</th>
<th>Output line voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td>11.68 %</td>
<td>1.63 %</td>
<td>105.81 %</td>
</tr>
<tr>
<td>Proposed</td>
<td>10.81 %</td>
<td>1.57 %</td>
<td>101.81 %</td>
</tr>
</tbody>
</table>
To compare the harmonic performance of the methods above, the FFT spectrum of common mode voltage $u_{com}$ and common mode current $i_{com}$ are shown in Fig. 10. As shown in Fig. 10(a), in the high frequency region which ranges from 10 kHz to 1 MHz, the main components of CMV are concentrated on the vicinity of switching frequency and its frequency multiplication. As observed, the high frequency components of proposed method are smaller than those of conventional method. Besides, the reduction of CMV would result in the reduction of CMC which is verified by Fig. 10(b). Thus, the adverse effects of EMI can be mitigated and the service life of motor can be extended.

Choosing the modulation index $m_v$ and output frequency as adjusting parameters and other conditions are the same with previous experiment, experimental data related to the RMS value of CMV and CMC under different parameters are summarized in Fig. 11. The decreasing trend in the RMS values with the increase of modulation index in the conventional method can be attributed to the usage of conventional zero vectors [14]. Under different output frequency, both these methods remain nearly constant because the CMC and CMV are mainly generated by high frequency components. Moreover, it can be noticed that the RMS values of the proposed method are lower.

To analyze the loss distribution of these two methods, the circuit is simulated in the PLECS-MATLAB environment. The simulated environment is the same with experimental specifications and the modulation index $m_v$ is fixed at 0.8 but load conditions are different. The corresponding results are depicted as Fig. 12. As shown, the conventional method has smaller power loss in the rectifier stage, but larger in the inverter stage. The power loss distribution of the proposed method is the opposite. Moreover, the total power loss of these two methods are nearly the same.

**IV. CONCLUSION**

In this letter, a new SVM method is proposed for IMC to reduce CMC. It is effective over the entire linear modulation range. The success of the method lies in introduction of new zero vectors. The new zero vectors would increase the common mode impedance. Thus, the peak value and high frequency components of CMC are attenuated. Moreover, complex
commutation process is not required and computation complexity has not increased which make it more suitable for practical application. Finally, this method is also applicable to other power converters which have similar structure with IMC.

REFERENCES


