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Single-phase current source converter with power decoupling capability using a series-connected active buffer

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Abstract: This study proposes a new power decoupling circuit applied to the single-phase current source converter (SCSC). Differing from the existing power decoupling technologies, the proposed power decoupling circuit could be viewed as a controlled voltage source in series with the DC inductor, and work with SCSC independently. That facilitates the separate design of the modulation schemes and the control algorithms for the power decoupling circuit and SCSC, and reduces the operation restrictions imposed by requirements. The fundamental principle of the proposed converter is analysed, and the voltage reference requirement for the buffer capacitor is investigated. To guarantee high input current quality of SCSC, a control method, where the input current is treated as a virtual control input, is proposed. Finally the effectiveness of this topology is verified by the simulations and experimental results.

1 Introduction

Recently, numerous DC loads, like light-emitting-diode (LED) lamps, DC sources, like fuel cells or PV panels and batteries in vehicle-to-grid (V2G) or uninterrupted power supplies (UPSs) have been increasingly used in power system. For a low power (<10 kW) system, usually single-phase AC/DC converters are required to exchange power with the AC grid. Unfortunately, the AC side instantaneous power is time-varying with twice the utility frequency [1]. As a result, the DC-link voltage/current contains a fluctuating component that changes at twice the line frequency [2]. The fluctuating component degrades the system performances because it introduces undesired harmonics into the AC side through the pulse width modulation [3, 4], reduces the maximum power point tracking (MPPT) efficiency of the photovoltaic (PV) panels [5, 6], generates low-frequency flicker of LED lamps [6, 7] and causes overheating of batteries [8–10].

The general method for mitigating the ripple power is to employ a large inductance or a bulky aluminium electrolytic (AE) capacitor. However, with this method it is difficult to obtain modularity and fast dynamic response. Moreover, the life expectancy of large AE capacitors is very limited. To meet the needs for high power density and long lifetime, a lot of active power decoupling methods has been proposed in [2, 11–18]. The fundamental principle is to divert the ripple power from DC-link to another energy storage component with long lifetime by an extra active circuit.

Usually, single-phase AC/DC converters are divided into voltage source converters and current source converters. In this paper, we are mainly concerned with the power decoupling techniques related to single-phase current source converter (SCSC). Over the past decades, the power pulsation decoupling methods for SCSC have been investigated [19, 20]. In [19], an *LC* parallel resonance circuit is inserted in the DC bus to prevent the DC-link ripple current with twice the utility frequency from flowing through the load. In [20], the authors proposed another decoupling concept of using balanced two-phase rectification, which increases the cost greatly. To reduce the cost, some decoupling circuits have been presented recently, see [3, 21, 22]. A common feature shared by them is that the proposed decoupling circuits consist of two insulated-gate bipolar transistors (IGBTs) (or metal–oxide–semiconductor field-effect transistor – MOSFET), two diodes and a buffer capacitor. Conversely, the distinctions lie in positions of the buffer capacitors in the topology. In [3, 21], the decoupling circuits are identical, while the difference is that the buffer capacitor in [21] plays the role of filtering besides storing ripple energy. In addition, the control method in [21] is more complicated compared with that in [3]. The presented topology of the power decoupling circuit in [22] is slightly different, as it is composed by adding a series-connected switch into each bridge arm, which means the operation restrictions are relaxed.

The aforementioned power decoupling circuits support bidirectional power flows. However, in many applications, only the inverter or rectifier operation is required. In this case, the active decoupling methods with low cost are presented [23, 24]. Ohnuma *et al.* [23] proposes an active buffer circuit consisting of one MOSFET and two diodes for the unity power factor inverter. In [24], an active buffer circuit consisting of two MOSFETs and one diode is proposed for the rectifier. However, in [23, 24], both of the active buffer capacitor voltages are higher than the peak value of the grid voltage. Hence, the voltage stresses of the semiconductors and the capacitors are relatively high, which results in considerable additional losses.

This paper presents a power decoupling method by using a series-connected active buffer (SAB). It could be viewed as a static synchronous series compensator to compensate the distorted rectifier's output voltage. With the proposed decoupling method, sinusoidal input current and low DC current ripple can be achieved under rectification state as well as inversion state. Compared with the existing active decoupling technologies in [3, 21, 22], the proposed power decoupling circuit works independently without being restricted by the switched state of the rectifier/inverter. Therefore its control is simple and the range of operation is wide. On the other hand, the voltages across the buffer capacitors are also different. The buffer capacitor voltages in [3, 21, 22] are controlled to be sinusoidal without the DC component. Thus, the voltage stresses of the associated switches are low. While the buffer capacitor voltages in [23, 24] must be higher than the peak values of the grid voltage, and the associated switching stress is higher. In the proposed method, the buffer capacitor voltage is between the two. Overall, the proposed power decoupling method is a good choice.

This paper is organised as follows: Section 2 introduces the topology and operation modes. Section 3 presents the operation principle of the proposed converter. Section 4 presents the modulation scheme and the associated control algorithm. Section 5

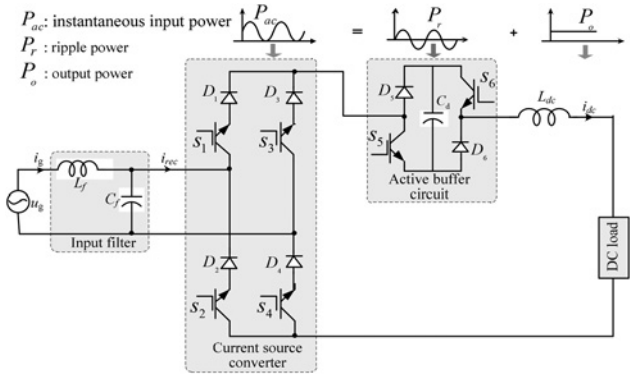

Fig. 1 *Topology of the proposed converter*

introduces the selection of the capacitor in SAB. Section 6 shows simulation and experiment results to validate the capabilities of the proposed converter. Finally, Section 7 concludes the paper.

2 Circuit topology

2.1 Circuit configuration

The topology of the proposed SCSC with power decoupling function is shown in Fig. 1. It is constructed by inserting a power buffer circuit to the DC bus of the conventional SCSC circuit. The buffer circuit consists of two switching devices (S_5, S_6), two diodes (D_5, D_6) and a capacitor (C_d). As can be seen, the power pulsation with twice the power supply frequency can be absorbed by the active buffer capacitor C_d. Consequently, the constant power feeds the DC load.

2.2 Operation modes

As shown in Fig. 2, four operation modes exist in SAB. In mode 1, S_5 is turned off and S_6 is turned on; while in mode 3, S_5 is turned on and S_6 is turned off. Both modes are equivalent in function, and the buffer capacitor is disconnected from the main circuit and the buffer circuit works as a freewheeling path. In mode 2, both S_5 and S_6 are turned off, then the buffer capacitor is charged and the excess energy provided by the grid is absorbed. In contrast, in mode 4, both S_5 and S_6 are turned on, then the buffer capacitor is discharged and the insufficient energy required by the DC load is supplemented.

3 Operation principle

Assume that the input voltage is sinusoidal with the amplitude V and angular frequency ω. It is expressed as

$$u_g = V\cos(\omega t) \tag{1}$$

The input current i_g is

$$i_g = I\cos(\omega t + \varphi) \tag{2}$$

where φ is the displacement angle and I is the amplitude of the input current.

Then the converter's instantaneous input power is expressed as

$$p_{ac} = \frac{1}{2}[VI\cos(\varphi) + VI\cos(2\omega t + \varphi)] \tag{3}$$

Obviously, a ripple power with twice the grid frequency exists in the input power. In most applications, the load consumes constant power. Thus, the ripple power must be buffered to avoid the distortion in the DC voltage/current and even the input current.

Therefore the capacitor in SAB should be controlled properly to absorb the ripple power in (3). If ignoring the power losses caused by semiconductor devices and the input filter, the following equation holds according to the power balance

$$\frac{1}{2}C_d u_d^2(t) - \frac{1}{2}C_d u_d^2(t_0) = \int_{t_0}^{t} \frac{VI\cos(2\omega t + \varphi)}{2}\mathrm{d}t \tag{4}$$

where u_d is the voltage of capacitor C_d. By integrating both sides of (4) with respect to time, then

$$u_d^2 = \bar{u}_d^2 + \frac{VI}{2\omega C_d}\sin(2\omega t + \varphi) \tag{5}$$

where

$$\bar{u}_d = \sqrt{u_d^2(t_0) - \frac{VI}{2\omega C_d}\sin(2\omega t_0 + \varphi)}$$

Recalling that u_d is positive, we obtain

$$u_d = \sqrt{\bar{u}_d^2 + \frac{VI\sin(2\omega t + \varphi)}{2\omega C_d}} \tag{6}$$

It is clear that $\bar{u}_d$ is a degree of freedom, and it satisfies the following

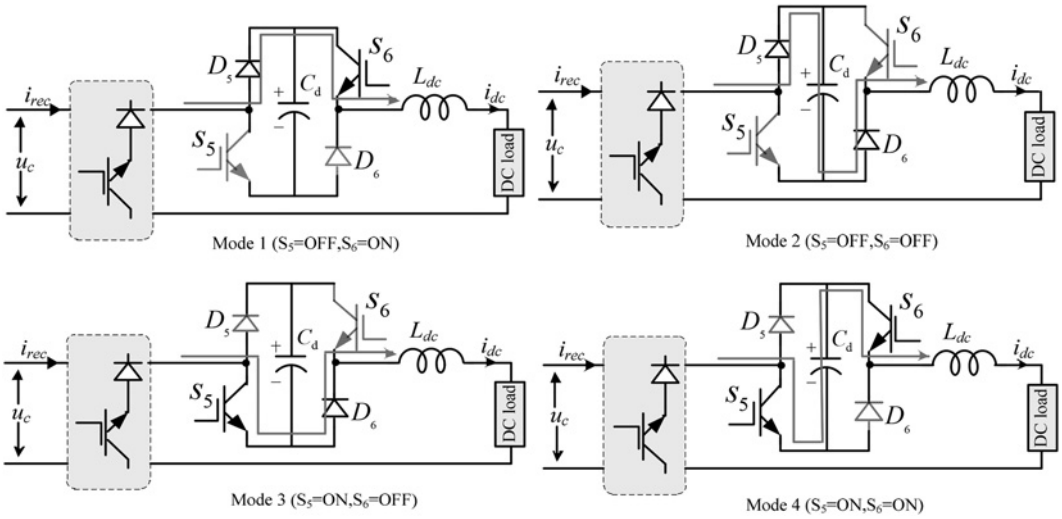

Fig. 2 *Operation modes of SAB*

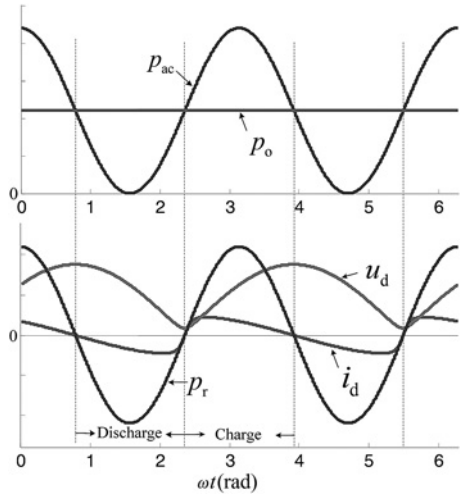

Fig. 3 *Operating waveforms*

constraint

$$\bar{u}_d \geq \sqrt{\frac{VI}{2\omega C_d}} \tag{7}$$

Moreover, the low-frequency capacitor current can be expressed as

$$i_d = \frac{VI\cos(2\omega t+\varphi)/2}{\sqrt{\bar{u}_d^2 + (VI\sin(2\omega t+\varphi)/(2\omega C_d))}} \tag{8}$$

For further showing the working principle, operating waveforms of the proposed converter are presented in Fig. 3. When the input power p_{ac} is larger than the output power p_o, the capacitor current i_d is positive and u_d increases, and the excess input power flows into the decoupling capacitor. When the AC side cannot feed the load adequate energy, the capacitor current i_d is negative and u_d decreases, then insufficient part is provided by the decoupling capacitor.

4 Modelling and control

4.1 Modelling

According to Fig. 1, the average model of the proposed converter is formulated as follows

$$L_f\frac{di_g}{dt} = u_g - u_c \tag{9}$$

$$C_f\frac{du_c}{dt} = i_g - i_{rec} \tag{10}$$

$$L_{dc}\frac{di_{dc}}{dt} = d_r u_c - d_d u_d - u_{dc} \tag{11}$$

$$C_d\frac{du_d}{dt} = i_{dc}d_d \tag{12}$$

$$i_{rec} = d_r i_{dc} \tag{13}$$

$$d_r = d_1 - d_2 \tag{14}$$

$$d_d = 1 - d_5 - d_6 \tag{15}$$

where u_c is the terminal voltage of capacitor C_f, u_{dc} is the voltage across the DC load, i_{dc} is the DC current flowing through inductor L_{dc} and d_i is the duty ratio of switch S_i ($i \in \{1, 2, \ldots, 6\}$). From (13), d_r is used to control input current and proportional to the desired input current in steady state. d_d is used to control SAB and proportional to the series compensating voltage for a constant u_d. Moreover, both d_r and d_d are defined on the interval $[-1, 1]$.

4.2 Controller design

To complete the power decoupling, based on the above results, the capacitor voltage u_d is controlled to track its reference as shown in (6) accurately. According to (12), d_d is selected as follows

$$d_d = \frac{C_d}{i_{dc}}[\dot{u}_d^* + k(u_d^* - u_d)] \tag{16}$$

where u_d^* is the reference of u_d and $\dot{u}_d^*$ is the time derivative of u_d^*, which serves as a forward compensation in the control. Substituting (16) into (12), then

$$\dot{e}_d = -ke_d \tag{17}$$

where $e_d = u_d^* - u_d$, and $k > 0$. It is clear that e_d convergences to zero asymptotically and the power decoupling is realised as well.

In [25, 26], different control methods were proposed to achieve constant DC voltage and sine input current irrespective of large ripples in the DC inductor current. However, in this paper, the control objectives are to achieve a given constant DC current and the sinusoidal grid current. The former is accomplished by the control of the SAB and the latter by the control of the SCSC which will be discussed in the following subsection.

Both sides of (11) are multiplied by i_{dc}, then yields

$$\frac{L_{dc}}{2}\frac{dx}{dt} = i_{rec}u_c - P_r - P_o \tag{18}$$

where $x = i_{dc}^2$, $P_r = i_{dc}u_d d_d$ and $P_o = i_{dc}u_{dc}$.

To obtain the sinusoidal grid current, the following equation should be satisfied in steady state

$$i_{rec} = I\cos(\theta+\varphi) \tag{19}$$

where θ is the phase of u_c, which is obtained by the digital phase-locked loop. I is the control input, which will be designed latter.

If ignoring the effect of the input filter, u_c could be approximated to $V\cos(\theta)$. By substituting (19) into (18), one has

$$\frac{L_{dc}}{2}\frac{dx}{dt} = \frac{1}{2}IV[\cos(\varphi) + \cos(2\theta+\varphi)] - P_r - P_o \tag{20}$$

The right-hand side of (20) is a periodic function. To facilitate the design of the controller, the periodic averaging method [27] is used here.

The average differential equation is as following

$$L_{dc}\frac{d\bar{x}}{dt} = IV\cos(\varphi) - 2P_o \tag{21}$$

where $\bar{x}$ is obtained by a moving average filter in implementation. Equation (21) is a linear first-order differential equation, and the control law for I, is designed as

$$I(s) = \left(k_p + \frac{k_i}{s}\right)(x^*(s) - \bar{x}(s)) \tag{22}$$

The overall control block diagram is shown in Fig. 4. Note that the DC current i_{dc} as shown in Fig. 4 appears in the denominator. Therefore, it results in singularity during starting up, which could be avoided by replacing it with its reference value during startup.

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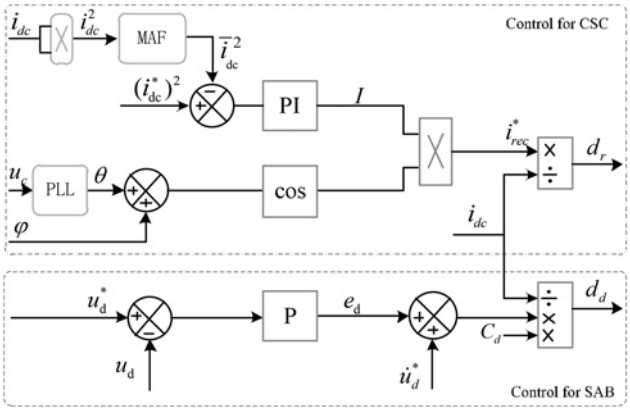

Fig. 4 *Block diagram of the control scheme*

4.3 Modulation strategy

To ensure the minimum switching loss with a fixed switching frequency, the combination of switches is restrained further as follows: if $d_r > 0$, $d_1 = 1$; otherwise, $d_1 = 0$. If $d_d > 0$, $d_6 = 0$; otherwise, $d_6 = 1$. The duty ratio of each switch is determined as shown in Table 1. To reduce current ripple, a symmetric switching pattern is applied. Fig. 5 illustrates the algorithm flowchart of the proposed modulation strategy for SCSC and SAB. The fourth block in Fig. 5 is designed to avoid the narrow pulse problem when d_r and d_d are sufficiently large or small. A simple way is to limit d_r and d_d in the interval $[\varepsilon, 1-\varepsilon]$, and ε is a small positive constant specified by designers. P_i ($i \in \{1, 2, \ldots, 6\}$) is the control signal for the switch S_i($i \in \{1, 2, \ldots, 6\}$). And $P_i = 1$ means that the S_i is turned on and $P_i = 0$ indicates that S_i is turned off. As can be observed in Fig. 5, for safe current commutation, overlap times are inserted. To further reduce the DC current ripple, the switching sequences of SAB are different under charging and discharging modes.

Table 1 Duty ratio of each switch

u_g	d_1	d_2	d_3	d_4	d_d	d_5	d_6
$u_g > 0$	1	$1 - d_r$	0	d_r	$d_d > 0$	$1 - d_d$	0
$u_g < 0$	0	$-d_r$	1	$1 + d_r$	$d_d < 0$	$-d_d$	1

5 Selection of the buffer capacitor in SAB

For simplicity, assume that the converter operates at unity input power factor. According to previous analysis, in steady-state variables d_d and d_r are expressed as

$$d_r = I\cos(\omega t)/i_{dc} \tag{23}$$

$$d_d = u_{dc}\cos(2\omega t)/u_d \tag{24}$$

Actually, the constraint for $\bar{u}_d$ in (7) is not sufficient in this study. Considering the requirement of the volt-second balance, d_d in (24) needs to be not more than one. Combining (6) with (24), the following inequality is obtained

$$\left|u_{dc}\cos(2\omega t)\right| \sqrt{\bar{u}_d^2 + \frac{VI\sin(2\omega t + \varphi)}{2\omega C_d}} \le 1 \tag{25}$$

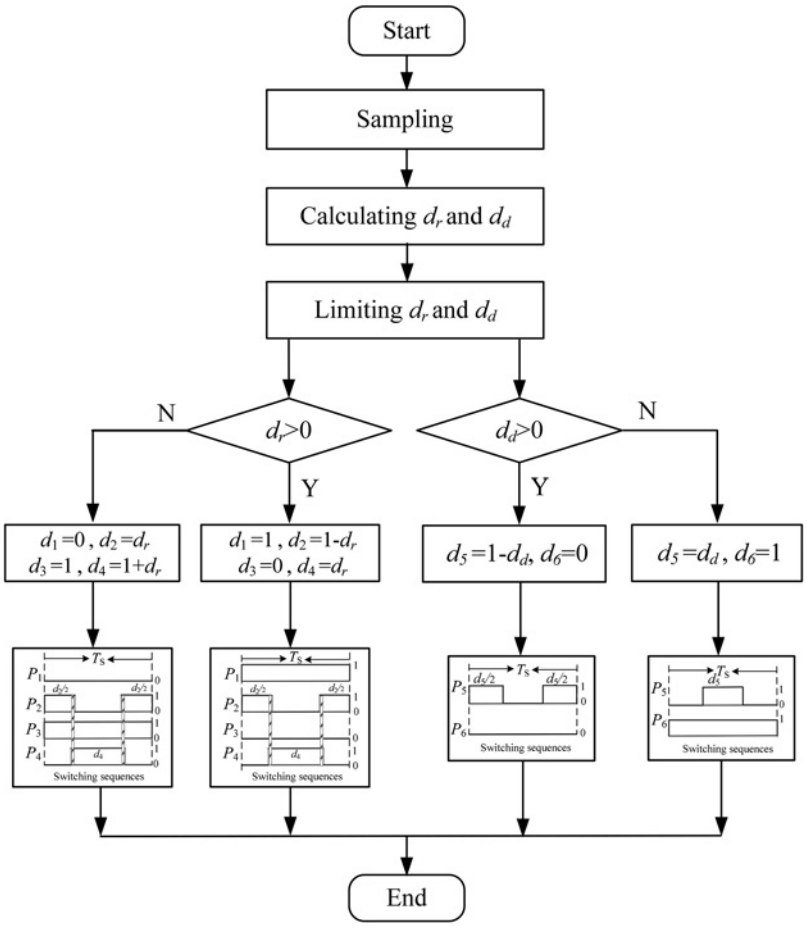

Fig. 5 *Flowchart of the proposed modulation strategy*

Table 2 Main parameters

Parameters	Variables	Value
amplitude of input phase voltage	V	92 V
grid angular frequency	ω	314 rad/s
input filter inductor	L_f	0.6 mH
input filter capacitor	C_f	20 μF
DC inductor	L_{dc}	3 mH
DC current reference	i_{dc}^*	4 A
DC side	R load/battery	8.7 Ω/36 V
switching frequency	f_s	20 kHz

By neglecting the power losses, VI can be replaced by $2P_o$. According to (7) and (25), the constraints of $\bar{u}_d$ are expressed as follows

$$\begin{cases} -u_{dc}^2\left[\sin(2\omega t)+\dfrac{1}{2\omega C_d}\dfrac{P_o}{u_{dc}^2}\right]^2+\left(\dfrac{P_o}{2\omega C_d u_{dc}}\right)^2+u_{dc}^2\le \bar{u}_d^2 \\ \bar{u}_d^2\ge \dfrac{P_o}{\omega C_d} \end{cases} \quad (26)$$

$\bar{u}_d$ is simplified further, yields

$$\bar{u}_d \ge \begin{cases} \sqrt{\dfrac{P_o}{\omega C_d}} & \dfrac{1}{2\omega C_d}\ge\dfrac{u_{dc}^2}{P_o} \\ \sqrt{u_{dc}^2+\dfrac{P_o^2}{4\omega^2 C_d^2 u_{dc}^2}} & \dfrac{1}{2\omega C_d}<\dfrac{u_{dc}^2}{P_o} \end{cases} \quad (27)$$

Obviously, increasing the capacitance of C_d can decrease the maximum capacitor voltage.

The main experimental parameters are listed in Table 2. Fig. 6 shows variation of the maximum capacitor voltage u_{dmax} as a function of the capacitor when the output power is 139.2 W. The selection of the buffer capacitor is a tradeoff between u_{dmax} and the cost of the capacitor. In this paper, a capacitor, whose detected capacitance value is 91.8 μF, is employed. With proper margin $\bar{u}_d$ is selected to be 80 V, and then the maximum capacitor voltage is 106.4 V according to (6).

6 Simulation and experimental results

6.1 Simulation results

The proposed topology is verified in Matlab/simulink environment. The simulation results are shown in Fig. 7. At the beginning, the decoupling circuit is not activated and the voltage of the decoupling capacitor is zero. Owing to a small capacitance of the DC inductor, the DC current i_{dc} is almost rectified sine shape.

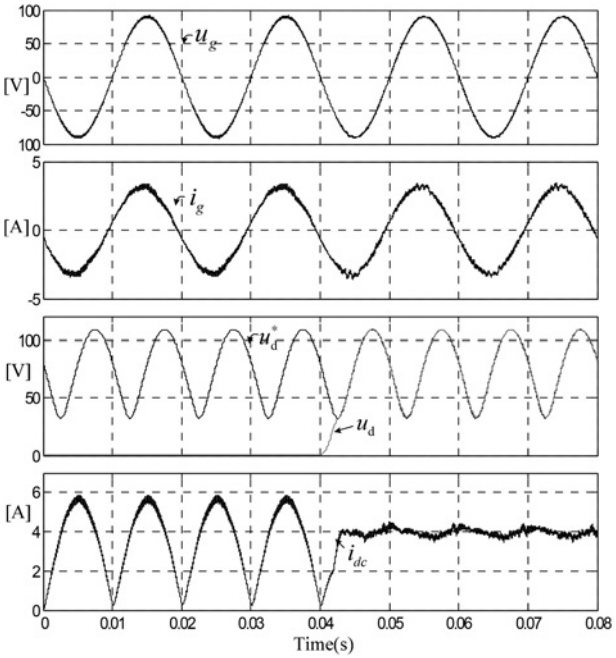

Fig. 7 *Simulation waveforms*

After the decoupling circuit is activated, the voltage of the decoupling capacitor tracks its reference quickly, and the DC current is a constant with a small fluctuation. As can be observed, the input current is always sinusoidal, and keeps in phase with the input voltage roughly.

The power losses are evaluated by the circuit simulator piece-wise linear electrical circuit simulation. The efficiency curves are illustrated in Fig. 8. η_1 is the overall conversion efficiency and η_d is the efficiency of the added decoupling circuit. Power losses caused by the SAB are around one-third of the whole. By power analyser, the measured efficiency is 84%, which is slightly smaller than the simulation results as the losses caused by the passive components are taken into consideration in experiments.

6.2 Experimental results

A prototype for the proposed converter is built in the lab for experimental verification. The schematic diagram of the single-phase current-source converter with SAB is shown in Fig. 1.The IGBTs used in the main circuit are 1MBH60D-100; the control of the converter was realised by a combination of the digital signal processor TMS320F28335 and the field-programmable gate array EP2C8T144C8N. The voltage of the battery load is 36 V, which is composed by three series battery

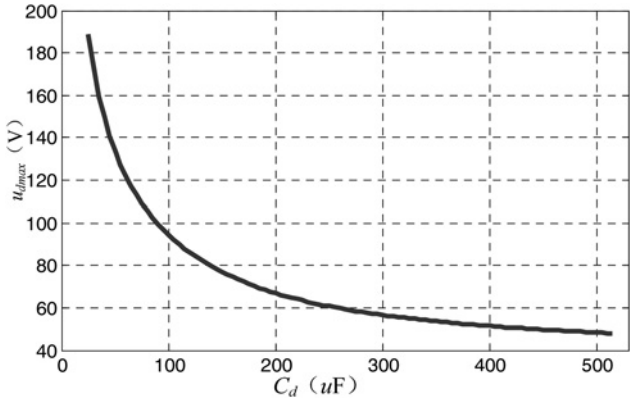

Fig. 6 *Maximum capacitor voltage against the capacitance capacity*

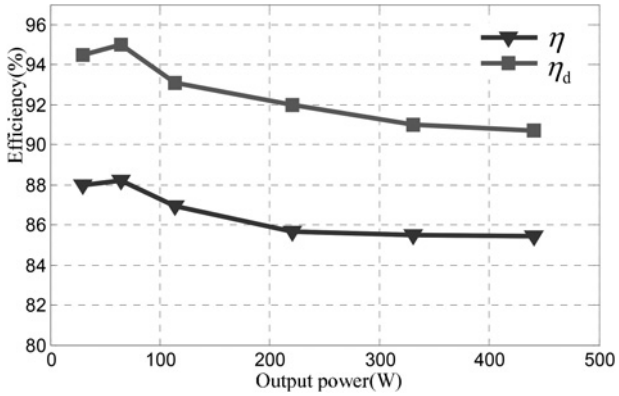

Fig. 8 *Efficiency curves of the proposed single-phase converter*

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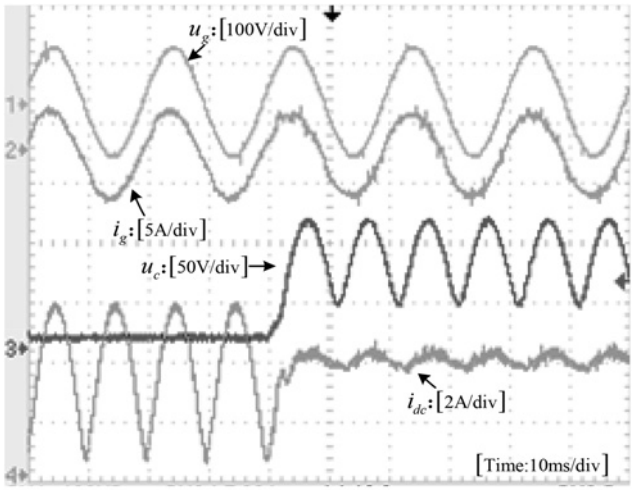
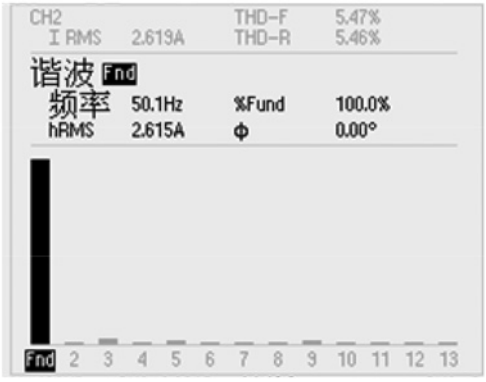


a



b

Fig. 9 *Experimental results with resistance load*

a Experimental waveforms
b Spectral analysis of the steady-state input current with decoupling circuit being activated

blocks at rated value 12 V/20 AH. To verify the performance of this topology and its related algorithm, two experiments are conducted.

In the first experiment, the load is a resistor of 8.7 Ω. With the proposed decoupling circuit being disabled, the converter works as a conventional SCSC. As illustrated in Fig. 9*a*, the DC current contains a large ripple at twice the frequency of the grid voltage. Once the decoupling circuit is activated, the current ripple is reduced greatly and the DC current is approximately a constant, which are in accord with the simulation results. In the identical situations, if a passive filter is used, it requires a large inductor of 110.8 mH to reach such a low-current ripple level. It also can be seen that the input current is sinusoidal and the power factor correction (PFC) is 0.97. Harmonic spectrum of the input current is illustrated in Fig. 9*b*. Moreover, Fig. 10 shows the total

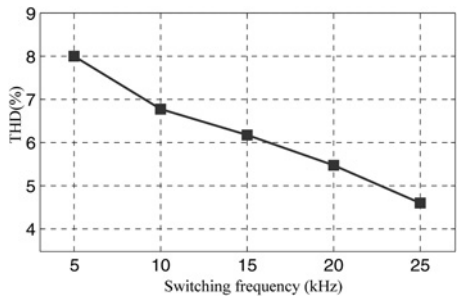


Fig. 10 *THDs of the input current against the switching frequencies*

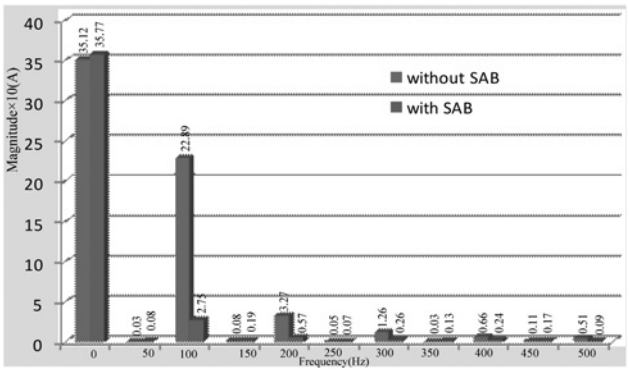
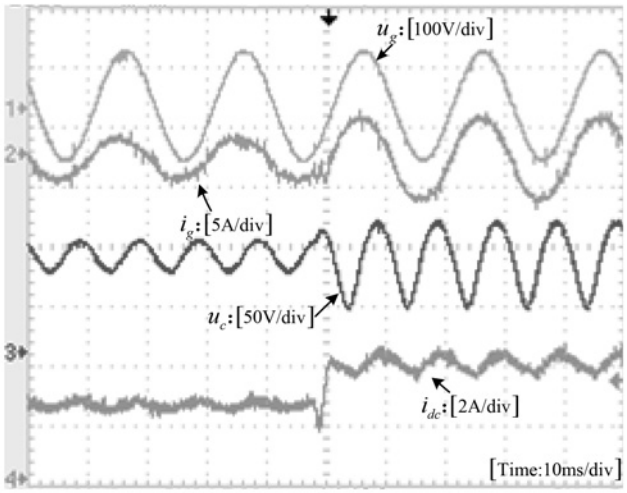


Fig. 11 *Spectral analysis for the DC bus current*

harmonic distortions (THDs) of the input current with different switching frequencies. Obviously, increasing switching frequency can improve the input current quality, but it leads to increasing the power losses as well. Under the tradeoff between them, 20 kHz is used in the experiment.

Fig. 11 shows the spectral analysis of the DC bus current under both conditions mentioned above, where the magnitude is multiplied by ten. Owing to the effectiveness of the proposed



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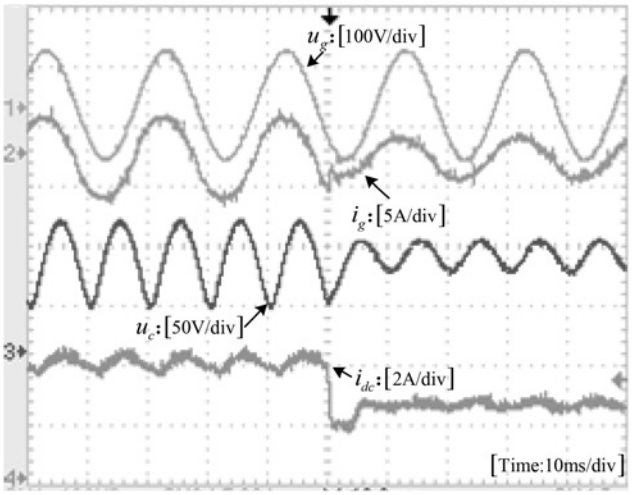

b

Fig. 12 *Experimental waveforms with DC current reference changing abruptly*

a From 2.5 to 4 A
b From 4 to 2.5 A

decoupling circuit, the second-order component in the DC bus current is reduced to be 12.01% of that in the conventional SCSC. And other low-frequency harmonic components are also much smaller compared with those in the conventional SCSC.

To show the dynamic response of the proposed topology, the experiments with step references were conducted. As shown in Fig. 12*a*, when the DC current reference increases from 2.5 to 4 A abruptly, the DC bus current tracks its reference immediately, the resulting voltage across the buffer capacitor become larger. Fig. 12*b* demonstrates the test results of stepping down the DC current reference. In both cases there is no obvious distortion in the grid current.

Battery loads are widely applied in the electric vehicle, UPS and so on. Thus the second experiment is conducted to verify the effectiveness of the proposed converter under the battery load condition. Fig. 13*a* illustrates the experimental results when charging the battery. As can be seen, i_{dc} is approximately a constant and the input current is sinusoidal and Fig. 13*b* shows the results of the proposed converter under inversion state. It is clear that the grid current and the grid voltage are phase reversal. Owing to complex battery characteristics, the input current with the battery load is worse than that with the resistance load. The THD is 7.2%/7.7% and the PFC is 0.96/0.95 under charging/discharging.

Sometimes converters are required to provide ancillary services such as reactive power and voltage support. Fig. 14 shows the waveforms when the converter has a power factor of 0.866, that is, $\varphi = \pm 30°$. This function is absent in [22, 23].

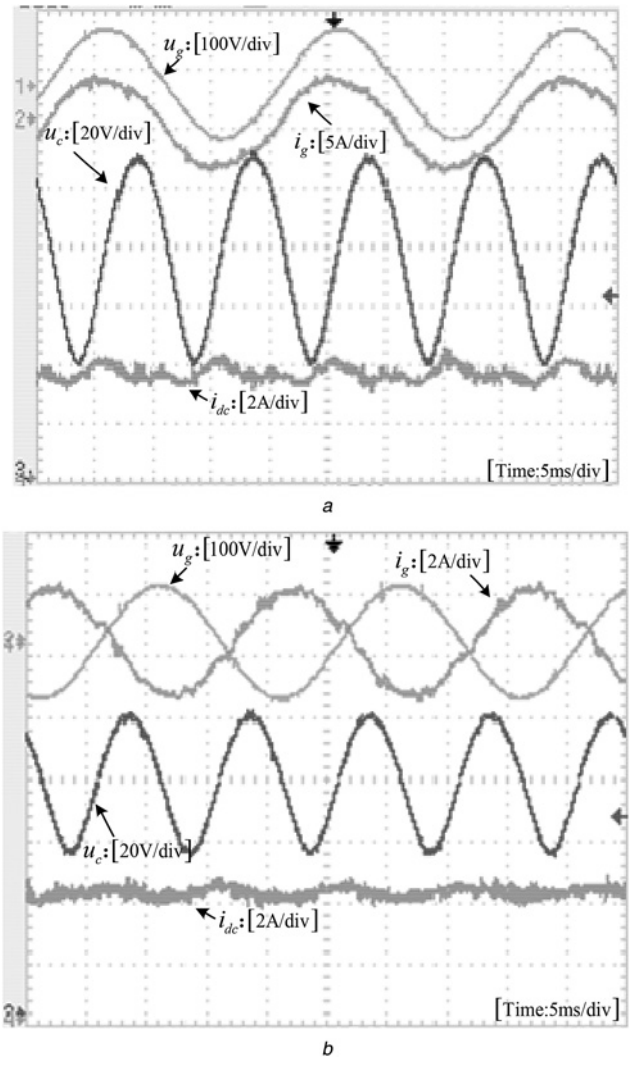

Fig. 13 *Experimental waveforms with a battery load*

a Rectification state
b Inversion state

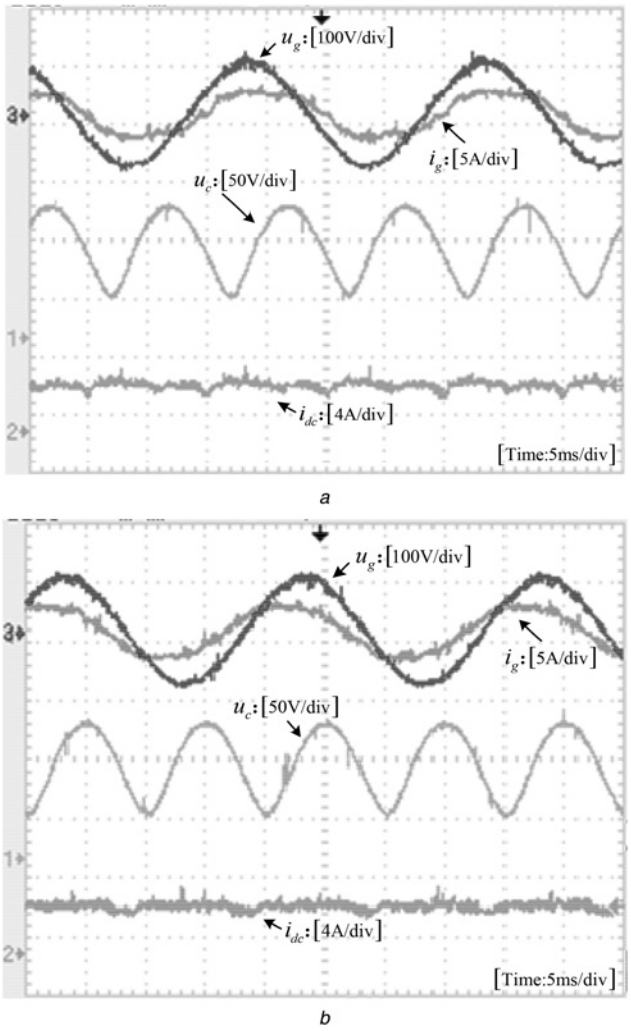

Fig. 14 *Experimental waveforms with $\varphi = \pm 30°$*

a $\varphi = -30°$
b $\varphi = 30°$

7 Conclusion

This paper presents a SCSC with power decoupling capability using an SAB. It works under rectification state as well as inversion state. With the proposed converter, the sinusoidal grid current and low-ripple DC current are achieved. The capacitor used in the SAB can be a film capacitor with a low rated voltage, which extends life and reduces the size and the weight. The proposed decoupling technology has reduced the presence of second harmonic current ripple by 87.99% with the proposed control method where the control reference is the buffer capacitor voltage. The proposed converter is suitable for single-phase rectifiers, UPS, V2G and the PV generation system. The validity of the proposed converter and control strategy was confirmed experimentally.

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