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Active power compensation method for single-phase current source rectifier without extra active switches

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Yonglu Liu, Yao Sun ✉, *Mei Su*

School of Information Science and Engineering, Central South University, Changsha, People's Republic of China
✉ *E-mail: yaosuncsu@gmail.com*

Abstract: The existing active power decoupling methods for single-phase current source rectifiers (SCSRs) usually involve a lot of additional semiconductor devices or energy storage units, which is adverse to cost and efficiency. This study proposes an active power decoupling method to buffer the double-frequency ripple power. The main circuit is configured by adding only a decoupling capacitor and a diode to the traditional SCSR. Compared with the existing ones, the added components are minimised. The operating principle and modulation scheme are described. A closed-loop control method is developed to enhance twice the line frequency ripple power compensation performance. The guide for the selection of the decoupling capacitance is also discussed. Simulations and experimental results are presented to show the effectiveness of the method.

1 Introduction

With the development of power electronic technology, more and more applications involve single-phase power system. For example, in distributed power generation the energy which comes from photovoltaic (PV) panels, fuel cells or others is transferred to utility grid by single phase grid-connected inverters [1, 2]. The residential and industrial power supplies, electric vehicles with low power level [3], and lighting system [4] are powered by single-phase power system. However, the inherent ripple power at twice the line frequency [5] in single phase power converters introduces some side effects, which degrades system performance and decreases reliability [6–12].

To address the issue above, the solutions can be categorised into passive method and active method. The passive method results from the standpoints of hardware. It also includes two types: increasing the dc-link capacitance or inductance [13] and making use of the LC resonant filters [14–16]. They are easy to implement, but large volume and weight are undesirable from the perspectives of costs and power density.

The active method is based on the principle of buffering the ripple power with small capacitors/inductors, which allow large voltage/current fluctuation. It can be further divided into two categories. One is implemented by swinging the dc-link bus voltage at twice the line frequency to buffer the ripple power [17–22]. It is usually carried out in two-stage single-phase inverters which consist of a front-end dc–dc converter and a downstream dc–ac inverter. The researches were mainly focused on maintaining the source current free from second ripple current [17–19] and dealing with the conflict between the dynamic response of dc-link voltage control and ac current quality [20, 21]. A distinct advantage of this method is that no extra circuit components are required. Its drawback consists in the limited applications (not suitable for single-stage power converters). In addition, since a second-order ripple voltage is superimposed on the dc bus, the voltage stress increases significantly, especially when the dc-link capacitance is small.

The other kind of active method is realised by adding an extra decoupling circuit. Recently this method has been extensively studied [23]. A variety of series and parallel compensation decoupling circuits [7, 24–32] are proposed to balance the power difference between the source and load. In the series compensation decoupling circuits [24, 25], the compensation voltage is injected to offset the pulsed voltage caused by the twice ripple power. In the parallel compensation decoupling circuits [7, 26–32] the compensation current is injected to prevent the pulsed current from flowing into the dc-link capacitor. However, a common drawback of the active methods is that an additional switching circuit is required, which leads to higher cost and power losses. Therefore, active methods sharing switches partially [33–40] and even entirely [41–44] between the decoupling and original circuits are proposed. The shared switches can be a bridge arm [33–36, 41, 42, 45, 46] or two upper/lower switches [37, 38]. However, the penalties for reducing switches may be the reduced voltage utility ratio, increased switches voltage stress and the increased complexity in modulation and control [31, 45, 47].

The decoupling circuits for CSCs are investigated relatively less compared with those tailored for VSCs. Most of them [25, 36, 38, 40] still require two additional active switches and two diodes even if switch sharing is applied. The open-loop control in which the decoupling capacitor voltage reference is taken as control objective was usually adopted [25, 36, 40]. As a result, excellent decoupling performance is difficult to achieve due to various unknown disturbances, for example, parameter drifts and grid harmonics. In [48] the proposed active method for SCSR needs no extra switches. However, two identical decoupling capacitors are needed to buffer the ripple power and the modulation scheme is also complicated. Moreover, voltage stress of the semiconductor devices increases.

A decoupling solution for SCSR without requiring additional active switches is proposed in this paper. The decoupling circuit only needs a decoupling capacitor and a protection diode, which is half the cost of that in [48]. Compared with the existing ones, the proposed one has advantages in cost and size. Meanwhile, the modulation algorithm is also easy to implement. To remove ripple power in the dc-link inductor completely a closed-loop control method is used. The rest of the paper is organised as follows: Section 2 introduces the proposed circuit configuration and switching states. Section 3 discusses the modulation scheme and control strategy. The selection of the decoupling capacitance is discussed in Section 4. Simulations and experimental results are proved in Section 5. Finally, the conclusions are made in Section 6.

2 Circuit configuration and switching states

2.1 Circuit configuration

Fig. 1 shows the proposed power decoupling circuit. It is formed by adding a decoupling capacitor C_d and a diode D_5 into the conventional SCSR. The second ripple power is diverted to C_d by

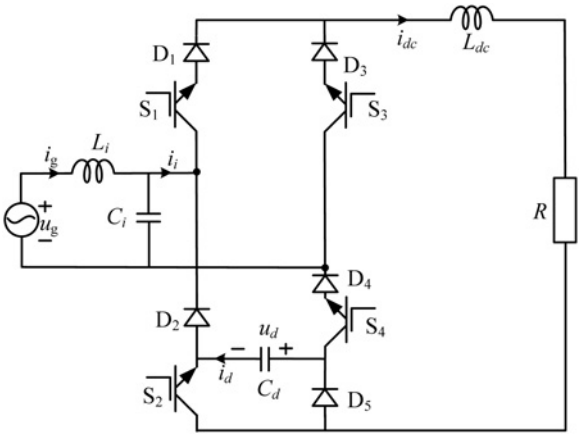

Fig. 1 *Proposed power decoupling circuit*

controlling switches S_2 and S_4 properly. Then the dc-link current i_{dc} can be kept constant even if a small inductor L_{dc} is used.

2.2 Switching states

In Fig. 1, S_1 and S_3 are complementary, whereas S_2 and S_4 do not obey that constraint. Fig. 2 illustrates six switching states, which are used in this paper. In the figures, $T=(S_1\ S_2\ S_3\ S_4)$ denotes the states of the four active switches, where $S_i=$ '1' ($i=1, 2, 3, 4$) indicates the corresponding switch is turned on and $S_i=$ '0' turned off. The switching states are divided into three groups in terms of functions. The first group includes the switching states 1 and 2, in which the ac side is connected to the dc-link current loop and the decoupling capacitor C_d is bypassed. This group contributes to synthesising the input current (transferring active power). The second group consists of switching states 3 and 4, in which the ac side is bypassed and the decoupling capacitor C_d works. This group is exclusively used to synthesise the decoupling capacitor current (buffer the ripple power). The third group is composed of switching states 5 and 6, which provide a freewheeling path for the dc-link current i_{dc}. The effects of different switching states on currents i_i and i_d are summarised in Table 1. The expected currents i_i and i_d can be synthesised by using the six switching states.

3 Modulation scheme and control strategy

3.1 Modulation scheme

To analyse the power flow of the proposed SCSR, the grid ac voltage u_g and current i_g are defined at first.

$$u_g = V\cos(\omega t) \tag{1}$$

$$i_g = I\cos(\omega t+\varphi) \tag{2}$$

where V and I are the amplitudes, ω is the angular frequency, and φ is the displacement angle. Then, the instantaneous power p_{ac} of the grid is expressed as

$$p_{ac} = u_g i_g = \underbrace{\frac{VI\cos(\varphi)}{2}}_{\bar{P}} + \underbrace{\frac{VI\cos(2\omega t+\varphi)}{2}}_{\tilde{p}}. \tag{3}$$

In most applications, the load consumes constant power $\bar{P}$. Hence, the ripple power $\tilde{P}$ should be buffered by the decoupling capacitor C_d. By ignoring the power losses, the decoupling capacitor voltage

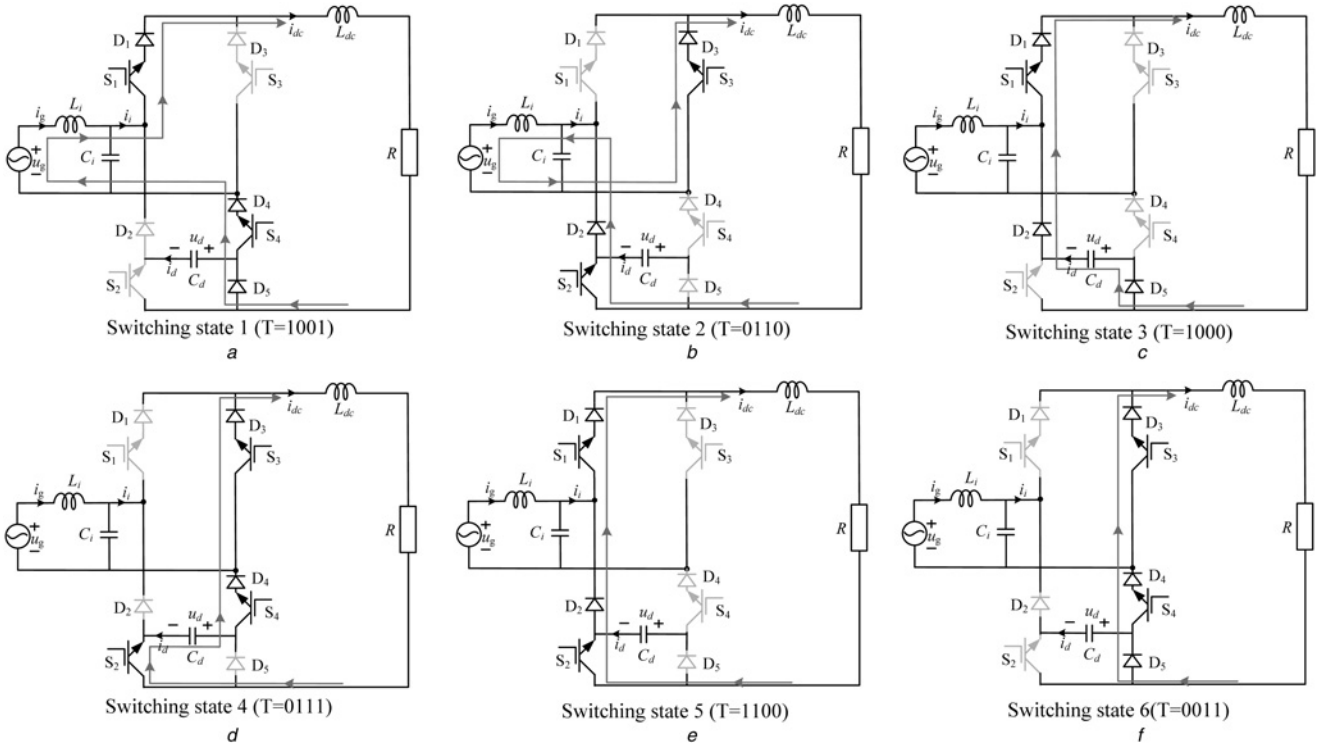

Fig. 2 *Switching states*

a Switches S_1 and S_4 are turned on, and switches S_2 and S_3 are turned off.
b Switches S_2 and S_3 are turned on, and switches S_1 and S_4 are turned off.
c Switch S_1 is turned on, and switches S_2, S_3, and S_4 are turned off.
d Switches S_2, S_3, and S_4 are turned on, and switch S_1 is turned off.
e Switches S_1 and S_2 are turned on, and switches S_3 and S_4 are turned off.
f Switches S_3 and S_4 are turned on, and switches S_1 and S_2 are turned off.

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Table 1 Switching states and currents

Switching states	i_i	i_d
1	i_{dc}	0
2	$-i_{dc}$	0
3	0	i_{dc}
4	0	$-i_{dc}$
5,6	0	0

u_d and current i_d can be expressed as [25]

$$u_d = \sqrt{\bar{u}_d^2 + \frac{VI\sin(2\omega t + \varphi)}{2\omega C_d}} \tag{4}$$

$$i_d = \frac{VI\cos(2\omega t + \varphi)/2}{\sqrt{\bar{u}_d^2 + \left(VI\sin(2\omega t + \varphi)/2\omega C_d\right)}} \tag{5}$$

where $\bar{u}_d$ is the dc component of u_d.

Assume that d_j ($j = 1, 2, 3, 4, 5, 6$) is the duty ratio of the switching state j, six duty ratios are subject to the following equation

$$\sum_{j=1}^{6} d_j = 1. \tag{6}$$

Then, i_i and i_d can be expressed as

$$\begin{bmatrix} i_i \\ i_d \end{bmatrix} = \begin{bmatrix} d_1 - d_2 \\ d_3 - d_4 \end{bmatrix} \cdot i_{dc}. \tag{7}$$

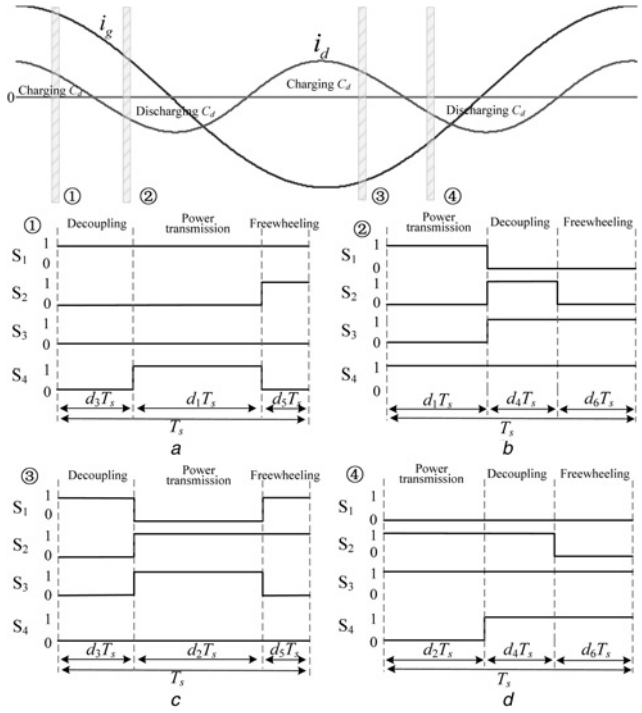

Fig. 3 *Switching patterns*

a Charging C_d when ac current is positive
b Discharging C_d when ac current is positive
c Charging C_d when ac current is negative
d Discharging C_d when ac current is negative

Substitute (3), (5), and (6) into (7), d_j can be expressed as

$$\begin{cases} d_1 = \begin{cases} i_{i\_ref}/i_{dc} & i_{i\_ref} > 0 \\ 0 & i_{i\_ref} \le 0 \end{cases} & d_2 = \begin{cases} 0 & i_{i\_ref} > 0 \\ -i_{i\_ref}/i_{dc} & i_{i\_ref} \le 0 \end{cases} \\ d_3 = \begin{cases} i_{d\_ref}/i_{dc} & i_{d\_ref} > 0 \\ 0 & i_{d\_ref} \le 0 \end{cases} & d_4 = \begin{cases} 0 & i_{d\_ref} > 0 \\ -i_{d\_ref}/i_{dc} & i_{d\_ref} \le 0 \end{cases} \\ d_5 = \begin{cases} 1 - \sum_{j=1}^{4} d_j & i_{d\_ref} > 0 \\ 0 & i_{d\_ref} \le 0 \end{cases} & d_6 = \begin{cases} 0 & i_{d\_ref} > 0 \\ 1 - \sum_{j=1}^{4} d_j & i_{d\_ref} \le 0 \end{cases} \end{cases} \tag{8}$$

where i_{i_ref} and i_{d_ref} are the references of the grid current and decoupling capacitor current, respectively. To reduce the dc-link current ripple, in each switching period T_s, the decoupling operation is first carried out when charging C_d; while the power transmission is prior when discharging C_d. To balance heat dissipation of each bridge, switching state 5/6 is carried out when charging/discharging C_d. Fig. 3 shows the switching patterns. From (8) and Fig. 3, it is easy for the modulation to be implemented in FPGA (CPLD).

3.2 Control strategy

According to Fig. 1, the equivalent averaged circuit model of the proposed converter is illustrated in Fig. 4. The averaged voltages u_r and u_c are provided by filter capacitor voltage and decoupling capacitor voltage, respectively. Then the differential equations of the converter are obtained as follows

$$L_i \frac{di_g}{dt} = u_g - u_c \tag{9}$$

$$C_i \frac{du_c}{dt} = i_g - i_i \tag{10}$$

$$L_{dc} \frac{di_{dc}}{dt} = u_r - u_s - Ri_{dc} \tag{11}$$

$$C_d \frac{du_d}{dt} = i_d \tag{12}$$

$$i_i = (d_1 - d_2)i_{dc} \tag{13}$$

$$i_d = (d_3 - d_4)i_{dc} \tag{14}$$

$$u_r = \frac{i_i}{i_{dc}} u_c = (d_1 - d_2)u_c \tag{15}$$

$$u_s = \frac{i_d}{i_{dc}} u_d = (d_3 - d_4)u_d \tag{16}$$

where i_g, i_{dc}, u_d are output variables; i_i and i_d are control input variables.

The precise open-loop reference (the decoupling capacitor voltage u_d or current i_d) for power decoupling is difficult to obtain due to

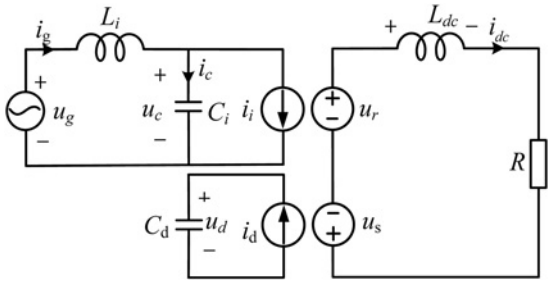

Fig. 4 *Equivalent averaged circuit*

power losses and parameter perturbations. To achieve good decoupling performance a closed-control strategy in [48] is adopted. Its basic idea is that i_d is responsive for regulating dc-link current i_{dc} and i_i is in charge of PFC as well as maintaining the dc component of the u_d at a given level.

3.2.1 Ripple power control: Actually, if the ripple power is not completely absorbed by the decoupling capacitor C_d, the residual part will be imposed on the dc-link inductor L_{dc}. Then the voltage-second balance will be broken and the dc-link current cannot be kept constant. Therefore, the error between the dc-link current reference and its detected value can be used to reflect the decoupling effect indirectly. As shown in Fig. 5, the error is sent to a proportional-integral (PI) controller. Then the reference i_{d_ref} can be obtained as follows

$$i_{d\_ref} = i_d + \frac{i_{dc}}{u_d} G_i(s)(i_{dc\_ref} - i_{dc}) \tag{17}$$

where i_d serves as a forward compensation in the control to improve the dynamic response.

3.2.2 Decoupling capacitor voltage control: The decoupling capacitor voltage fluctuates as a result of buffering the ripple power. Though the required average ripple power through C_d over a line frequency cycle is zero, the power losses due to switches and capacitors are unavoidable. Therefore, the dc component of the decoupling capacitor voltage should be maintained at a predetermined level. Before introducing the voltage control of C_d, assume the dc-link current subsystem is in steady state.

According to (11) and (15), u_s in steady state can be expressed as

$$u_s = \frac{i_i}{i_{dc}} u_c - R i_{dc}. \tag{18}$$

Substitute (15) and (18) to (12), the voltage dynamic of C_d is express as follows.

$$\frac{C_d}{2}\frac{dx}{dt} = u_c i_i - R i_{dc}^2 \tag{19}$$

where $x = u_d^2$. Clearly, the voltage across C_d can be controlled by control input i_i. By ignoring the effects of the input filters, $i_i \simeq i_g$ and $u_c \simeq u_g$, then (19) can be rewritten as

$$\frac{C_d}{2}\frac{dx}{dt} = \frac{VI}{2}\left[\cos(\varphi) + \cos(2\omega t + \varphi)\right] - R i_{dc}^2. \tag{20}$$

Since (20) is a periodic system, the periodic averaging method [49] is used to design the controller. Then the average differential equation of (20) is

$$C_d \frac{d\bar{x}}{dt} = VI\cos(\varphi) - 2R i_{dc}^2 \tag{21}$$

where $\bar{x} = \bar{u}_d^2 = (1/T)\int_{t-T}^{t} x(\tau)d\tau$, and $\bar{x}$ is obtained by a moving average filter in implementation. Equation (21) is a simple first-order system, thus $G_v(s)$ is achieved by a PI controller. Then the reference i_{i_ref} can be written as

$$\begin{aligned} i_{i\_ref} &= I_{\_ref}\cos(\omega t + \varphi) \\ &= \left\{I + G_v(s)(\bar{u}_{d\_ref}^2 - \bar{u}_d^2)\right\}\cos(\omega t + \varphi) \end{aligned} \tag{22}$$

where $I = 2\bar{P}/V$ is the feed-forward term to increase the dynamic response of the current control.

Fig. 5 shows the overall block diagram of the control scheme. It mainly includes a phase locking loop, a voltage controller and a current controller. Compared with the control scheme in [25], the complexity does not increase a lot. A highlight merit of the proposed control is the feed-back regulation of the dc-link current, which enhances the decoupling effects.

4 Design of the decoupling circuit

In this section, the values of $\bar{u}_d$ and C_d will be determined. There are two basic constraints imposed by the normal operation of the converter. One is that the decoupling capacitor voltage should be higher than the grid voltage. Then, the misgating-on of D_2 can be avoided when carrying out switching states 1 and 4. The other is that the synthesis of input current and decoupling current should be accomplished in each switching period, that is, $\sum_{j=1}^{4} d_j$ should be no more than unity. Hence, inequalities (23) and (24) should hold for any time

$$\sqrt{\bar{u}_d^2 + \frac{VI\sin(2\omega t + \varphi)}{2\omega C_d}} \geq \left|V\cos(\omega t)\right| \tag{23}$$

$$m\left(\left|\cos(\omega t + \varphi)\right| + \left|\frac{V\cos(2\omega t + \varphi)/2}{\sqrt{\bar{u}_d^2 + (VI\sin(2\omega t + \varphi)/2\omega C_d)}}\right|\right) \leq 1 \tag{24}$$

where $m = I/i_{dc}$ is the modulation index.

Assume that the converter works in unity power factor, the maximum grid current is I_m, and the required maximum modulation index is M.

On the basis of the assumptions above, (23) can be simplified as

$$\bar{u}_d \geq \sqrt{\frac{1}{2}\left(V^2 + \sqrt{V^4 + \left(\frac{VI_m}{\omega C_d}\right)^2}\right)} \tag{25}$$

Equation (24) can also be simplified as

$$M \leq \frac{1}{1 + \left(V/2\sqrt{\bar{u}_d^2 - (VI_m/2\omega C_d)}\right)} \tag{26}$$

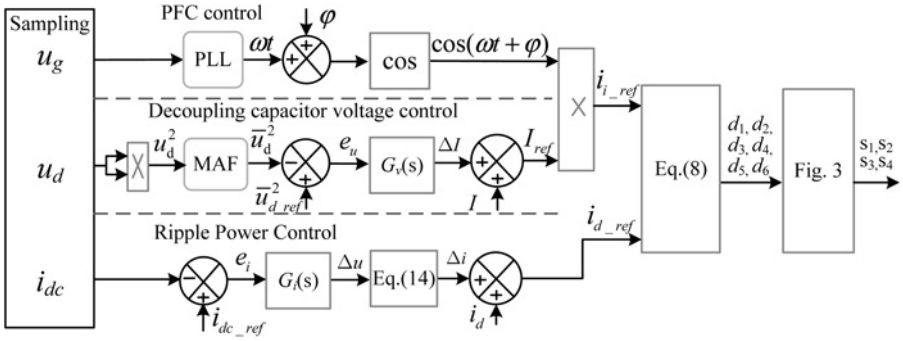

Fig. 5 *Block diagram of the control scheme*

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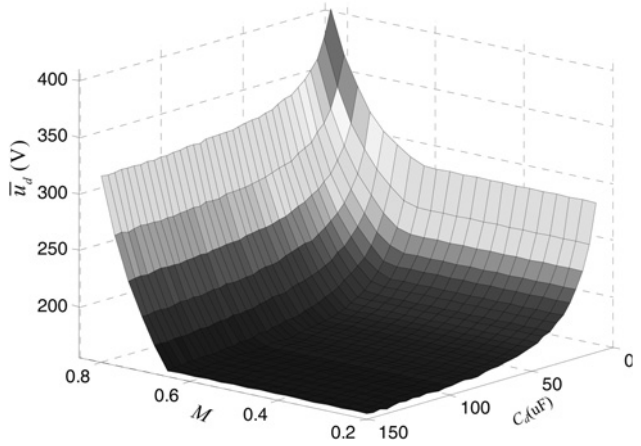

Fig. 6 *Decoupling capacitor voltage as a function of the decoupling capacitance and modulation index*

Table 2 Parameters used in analysis, simulation, and experiment

Parameters	Symbols	Values
input phase voltage	V	$110\sqrt{2}$V
source angular frequency	ω	314 rad/s
input filters	L_i/C_i	0.6 mH/20 μF
Dc filter inductor	L_{dc}	5 mH
active buffer capacitor	C_d	90 μF
load resistance	R	8.7 Ω
load power	P	217.5 W
switching frequency	f_s	20 kHz

Besides the constraints imposed by its normal operation, the maximum voltage stress on switches should be considered. Therefore,

$$\max(u_d) \leq u_p \tag{27}$$

where u_p denotes the maximum permissible voltage, (27) can be

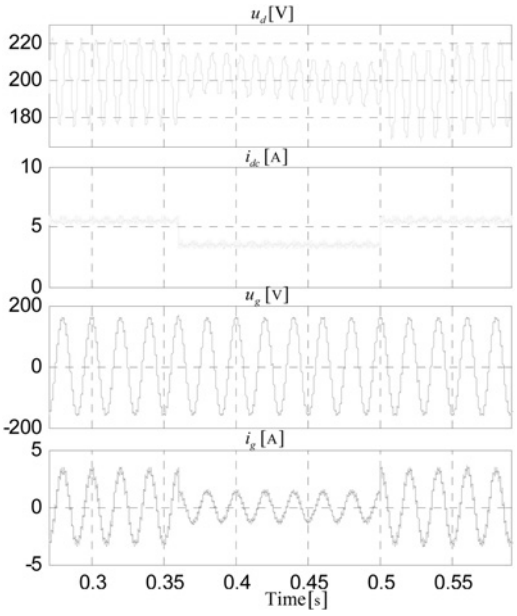

Fig. 7 *Simulation results*

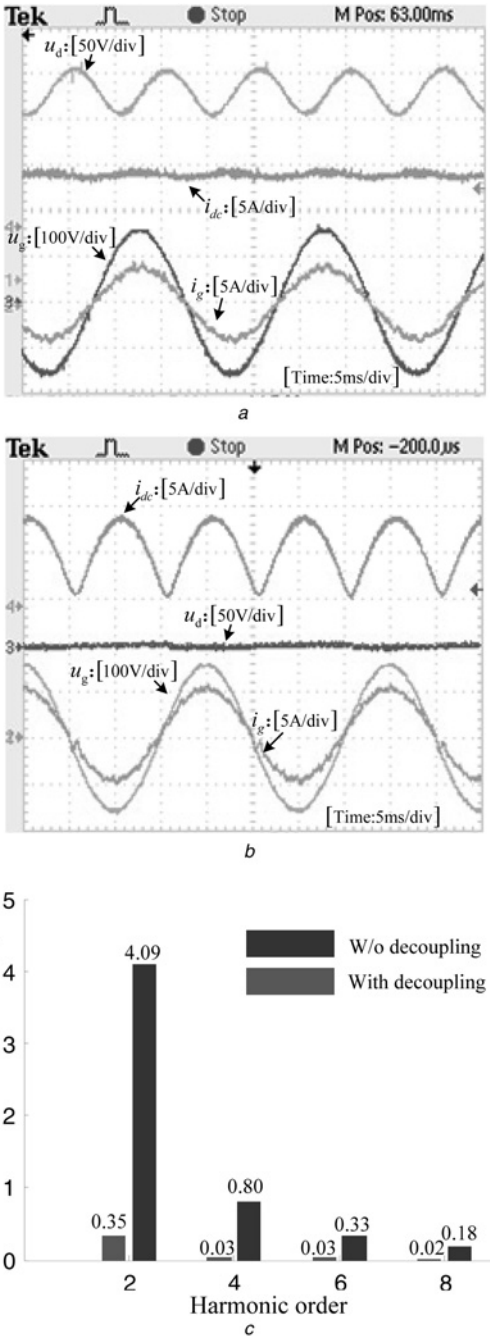

Fig. 8 *Steady-state experimental waveforms*

a With decoupling function
b Without decoupling function
c Spectral analysis for dc-link current

rewritten as

$$\sqrt{\bar{u}_d^2 + \frac{VI_m}{2\omega C_d}} \leq u_p \tag{28}$$

On the basis of inequalities (25), (26) and (28), a feasible region for $\bar{u}_d$ and C_d can be solved. Using the parameters in simulation and experiments, the relation between $\bar{u}_d$, C_d, and M is shown in Fig. 6. As can be seen, when M is small, $\bar{u}_d$ is not affected by M. Because (25) is the dominant constraint. However, when M is large, (26) becomes the dominant constraint. Therefore, $\bar{u}_d$ increases significantly with increasing M. On the other hand, increasing capacitance obviously can decrease $\bar{u}_d$. However, once C_d is beyond a certain value, increasing capacitance cannot

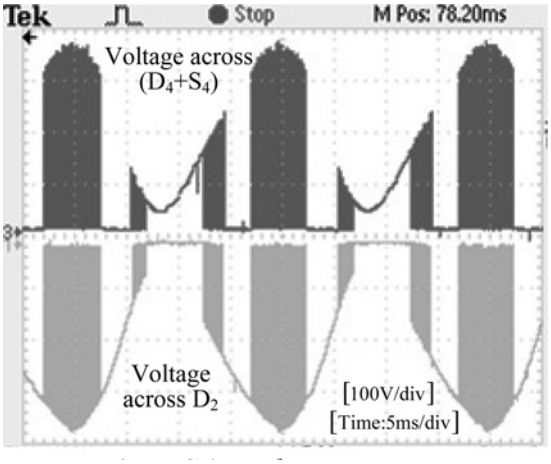

Fig. 9 *Experimental waveforms of voltages across $(D_4 + S_4)$ and D_2*

decrease $\bar{u}_d$ significantly. In this study, by making a trade-off between voltage stress and cost the decoupling capacitance is 90 μF and $\bar{u}_d$ is set to 200 V.

5 Simulations and experimental results

Simulation study is carried out in Matlab/Simulink environment and the circuit parameters are listed in Table 2. The waveforms in steady-state and transient operation are presented in Fig. 7. At beginning system operates in steady-state with a 5.4 A dc-link current. The step-down change of dc-link reference from 5.4 to 3.4 A and step-up change from 3.4 to 5.4 A happen at $t = 0.36$ and 0.5 s. As can be seen, the dc-link current i_{dc} is always smooth in both operation states because the ripple power is diverted to the decoupling capacitor C_d. Meanwhile, the low dc-link current ripple verifies the effectiveness of the designed switching patterns. The source current i_g is always sine shaped and in phase with the source voltage u_g.

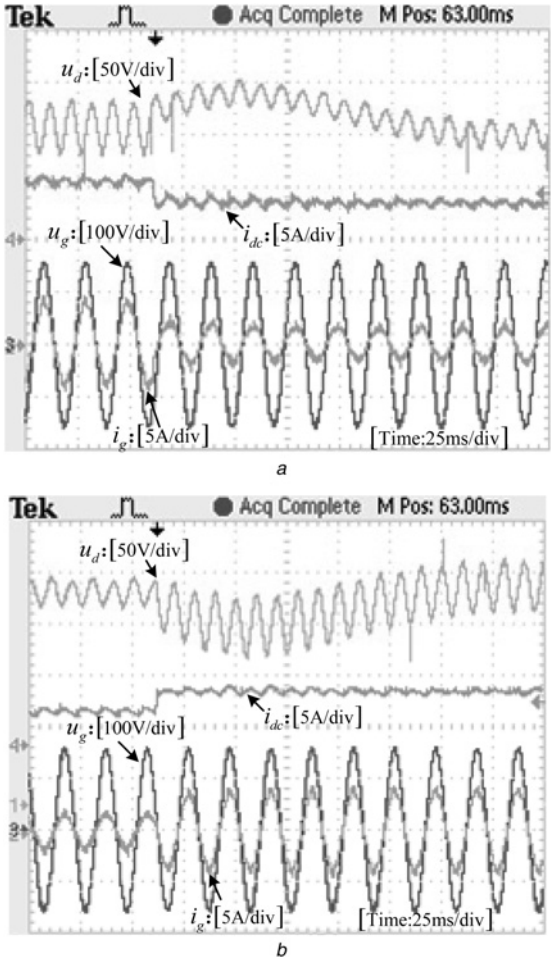

Fig. 10 *Dynamic experimental waveforms*

a 100% to 40% step-down load change
b 40% to 100% step-up load change

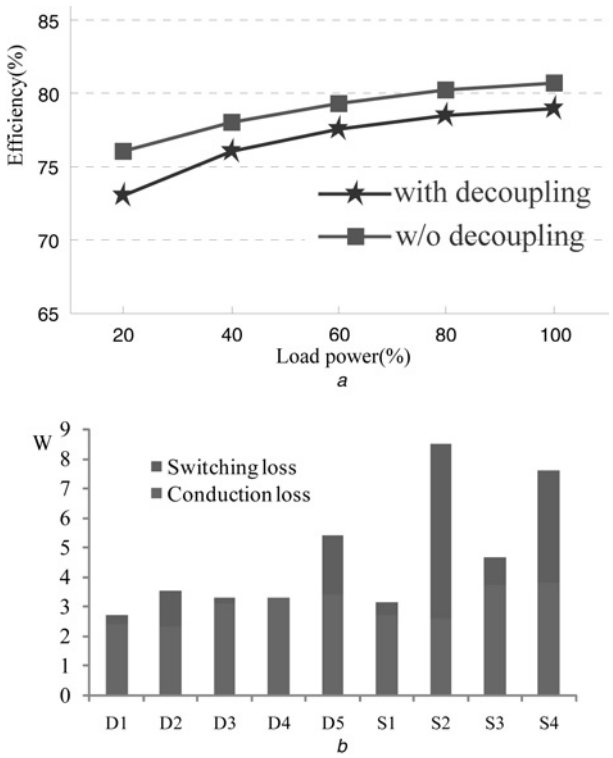

Fig. 11 *Power losses analysis*

a Efficiency comparison
b Loss distribution of the proposed converter with 100% load operation

A prototype was built to verify the feasibility of the decoupling topology and control schemes. The control algorithm of the converter is realised by a combination of digital signal processor TMS320F28335 and field programmable gate array FPGA EP2C8T144C8N. The decoupling capacitor is formed by connecting three 30 μF/490 V film capacitors in parallel. Fig. 8*a* shows the steady-state experimental waveforms. As can be seen, the experimental results are in good agreement with the simulation results. The THD of source current i_g is 4.63%, which meets the requirements of standard IEC/EN 61000-3-2 Class A. After disabling the decoupling function the twice ripple power will be imposed on the dc-link inductor immediately and the related experimental waveforms are shown in Fig. 8*b*. Clearly, the dc-link current fluctuates with twice the line frequency. The grid ac current is seriously distorted at the valley of the dc-link current. Fig. 8*c* shows the spectrum of the dc-link current with and without decoupling. It is clear that there is a dramatic reduction of the second harmonic current when activating decoupling function. Other low-frequency harmonic components are also reduced.

Fig. 9 shows the waveforms of voltages across $(D_4 + S_4)$ and D_2. As seen, the envelope of the voltage across $(D_4 + S_4)$ is $(u_g + u_d)$, which is always positive. Therefore, the reverse voltage across D_4 is negative during the turn-off process, which reduces the turn-off loss. The envelope of the voltage across D_2 is $(-u_g\text{-}u_d)$, which is always negative. Then D_2 can be blocked reliably when S_4 is in the on state. On the other hand, the voltage stress of S_4 and D_2 are the highest in all the semiconductor devices.

Fig. 10 shows the dynamic response of the system when the load power is subject to a 100% to 40% step-down change and a 40% to

100% step-up change. As can be seen, in Fig. 10*a* the dc-link current i_{dc} decreases from 5.4 to 3.4 A quickly due to the closed-loop control method. The excess energy in the dc-link inductor is transferred to the decoupling capacitor and the capacitor voltage level is raised. The decoupling capacitor voltage enters steady state relatively slow as results of low bandwidth of the voltage control loop. With the decrease of the load power, the ripple power is reduced and the fluctuation range of u_d decreases accordingly. Fig. 10*b* shows the opposite transient process. The experimental results also coincide with those in the simulation.

Fig. 11*a* illustrates the efficiency curves of the proposed converter and the conventional SCSR. As can be seen, the efficiency of the proposed converter is slightly lower than that of the conventional case. The main reason is the increased voltage stresses, which increases the switching power losses. As well known, all the active decoupling methods cause extra power losses. As reported in [6, 44], usually the efficiency penalty is more than two percentage points. However, in the proposed method the system efficiency drop under rated load power is 1.5%, which is lower than those reported in [25, 48]. Fig. 11*b* shows the estimated power loss distribution. Apparently, the switching losses of the semiconductor devices in the lower bridge arm are significant. As analysed previously, switching loss does not happen to D_4 because the reverse voltage across D_4 is negative.

6 Conclusion

An active ripple power decoupling method is proposed for SCSR to reduce the twice ripple power and the dc-link inductance. A highlight merit of the method is that the required extra components are minimised, which reduces cost and improves reliability. The operating principle has been analysed and a closed-loop control method is used to enhance the ripple power decoupling effects. Simulations and experimental results in both steady-state and transient operations are obtained. The results show that the proposed decoupling method reduces the second harmonic current by 91.4%, which reduces required dc-link inductance greatly. One shortcoming of the method is the increased switching voltage stress, which decreases the system efficiency inevitably. Thus, the efficiency optimisation will be studied in the future work.

7 Acknowledgments

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